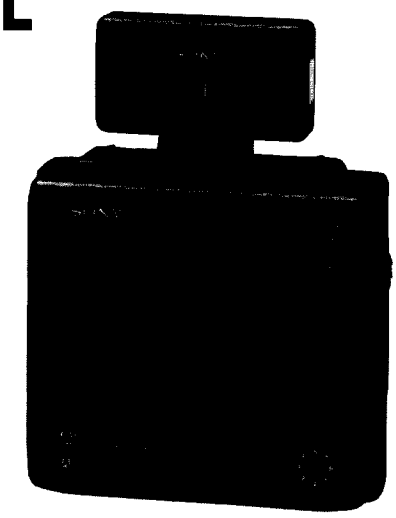
GPX-5

SERVICE MANUAL

AEP Model



Model Name Using Similar Mechanism	NEW
CD Mechanism Type	KSM-413AAA/J-N
Optical Pick-up Name	KSS-413A/J-N

SPECIFICATIONS

CD-ROM Player/GPS Aerial/LCD Monitor

Operating temperatures
–10°C to + 50°C
Power source DC 12 V car battery (negative ground)
Current drain Approx. 1.5 A
Input connectors
Headphones connector
Car mount adaptor connector
GPS connector

CD-ROM player

Format NAVIKEN-standard format

GPS aerial

Aerial Micro-strip flat type
Reception frequency
1,575.42 MHz (C/A code)
Reception system
Parallel 12 channels (capable of receiving signals from up to 12 satellites simultaneously)
Reception sensitivity
–130 dBm
Position updata rate
approx. 1 second

LCD monitor

Type LCD color monitor
Display Transparent TN LCD panel
System TFT active matrix system
Monitor size 5 inches, 101.6 × 74.7 mm
(w × h, diagonal measurement)
Segments 168,480 segments (234 × 720)

Connection box section

Inputs NAVI BUS cable
GPS aerial cord
Adaptor cable
Mains lead

Operating duration of lithium batteries

When playing CDs: approx. 150 minutes
When navigating: approx. 110 minutes

– Continued on next page –

HANDY NAVIGATION SYSTEM

MICROFILM

SONY®

Dimensions

CD-ROM player/LCD monitor
approx. 151.5 × 57 × 144 mm
not including projecting parts
Remote commander
approx. 38.6 × 35 × 167 mm
GPS aerial approx. 92 × 25 × 50 mm

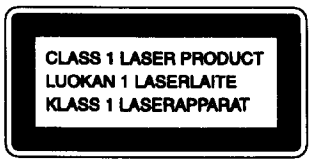
Mass

CD-ROM player/LCD monitor
approx. 900 g
Remote commander
approx. 140 g
GPS aerial approx. 200 g

Supplied Accessories

Remote commander RM-X58A (1)
Aerial cables 75 mm
67 cm
Carrying case (1)
Side pocket (1)

Design and specifications are subject to change without notice.



This appliance is classified as a CLASS 1 LASER product.
The CLASS 1 LASER PRODUCT MARKING is located on the rear exterior.

CAUTION

Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Flexible Circuit Board Repairing

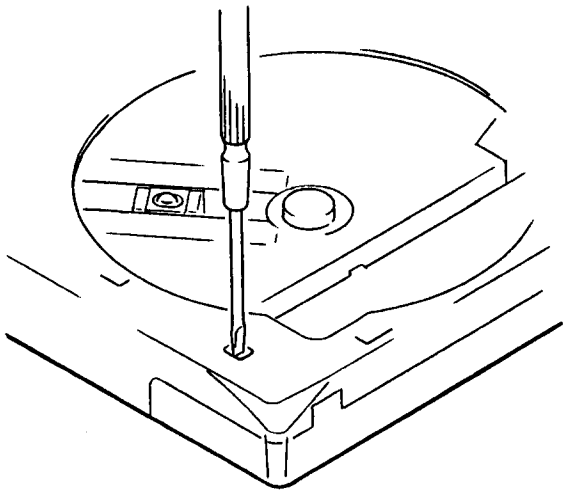
- Keep the temperature of the soldering iron around 270°C during repairing.
- Do not touch the soldering iron on the same conductor of the circuit board (within 3 times).
- Be careful not to apply force on the conductor when soldering or unsoldering.

Notes on Chip Component Replacement

- Never reuse a disconnected chip component.
- Notice that the minus side of a tantalum capacitor may be damaged by heat.

LASER DIODE AND FOCUS SEARCH OPERATION CHECK

1. Open the upper lid.
2. Push on OPEN SWITCH (S001) as following figure.
3. Confirm the laser diode emission while observing the objecting lens. When there is no emission, Auto Power Control circuit or Optical Pick-up is broken.
   Objective lens moves up and down once for the focus search.



NOTES ON HANDLING THE OPTICAL PICK-UP BLOCK OR BASE UNIT

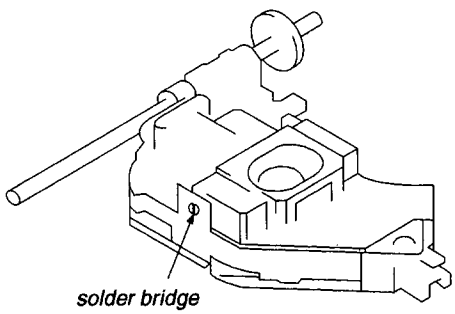
The laser diode in the optical pick-up block may suffer electrostatic breakdown because of the potential difference generated by the charged electrostatic load, etc. on clothing and the human body.
During repair, pay attention to electrostatic breakdown and also use the procedure in the printed matter which is included in the repair parts.
The flexible board is easily damaged and should be handled with care.

NOTES ON LASER DIODE EMISSION CHECK

The laser beam on this model is concentrated so as to be focused on the disc reflective surface by the objective lens in the optical pick-up block. Therefore, when checking the laser diode emission, observe from more than 30 cm away from the objective lens.

NOTES FOR REPLACEMENT OF MECHANISM DECK AND OPTICAL PICK-UP BLOCK

When replacing the mechanism deck and optical pick-up, solder bridge should be removed on the flexible board in the optical pick-up.



optical pick-up block

CAUTION

Danger of explosion if battery is incorrectly replaced.
Replace only with the same or equivalent type recommended by the equipment manufacturer.
Discard used batteries according to manufacture's instructions.

ADVARSEL!

Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering.
Udskiftning må kun ske med batteri
af samme fabrikat og type.
Lever det brugte batteri tilbage til leverandøren.

ADVARSEL

Eksplosjonsfare ved feilaktig skifte av batteri.
Benytt samme batteritype eller en tilsvarende
type anbefalt av apparatfabrikanten.
Brukte batterier kasseres i henhold til fabrikantens
instruksjoner.

VARNING

Explosionsfara vid felaktigt batteribyte.
Använd samma batterityp eller en likvärdig typ som rekommenderas av apparattillverkaren.
Kassera använt batteri enligt gällande föreskrifter.

VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu.
Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

SAFETY-RELATED COMPONENT WARNING!!

COMPONENTS IDENTIFIED BY MARK ⚠ OR DOTTED LINE WITH MARK ⚠ ON THE SCHEMATIC DIAGRAMS AND IN THE PARTS LIST ARE CRITICAL TO SAFE OPERATION. REPLACE THESE COMPONENTS WITH SONY PARTS WHOSE PART NUMBERS APPEAR AS SHOWN IN THIS MANUAL OR IN SUPPLEMENTS PUBLISHED BY SONY.

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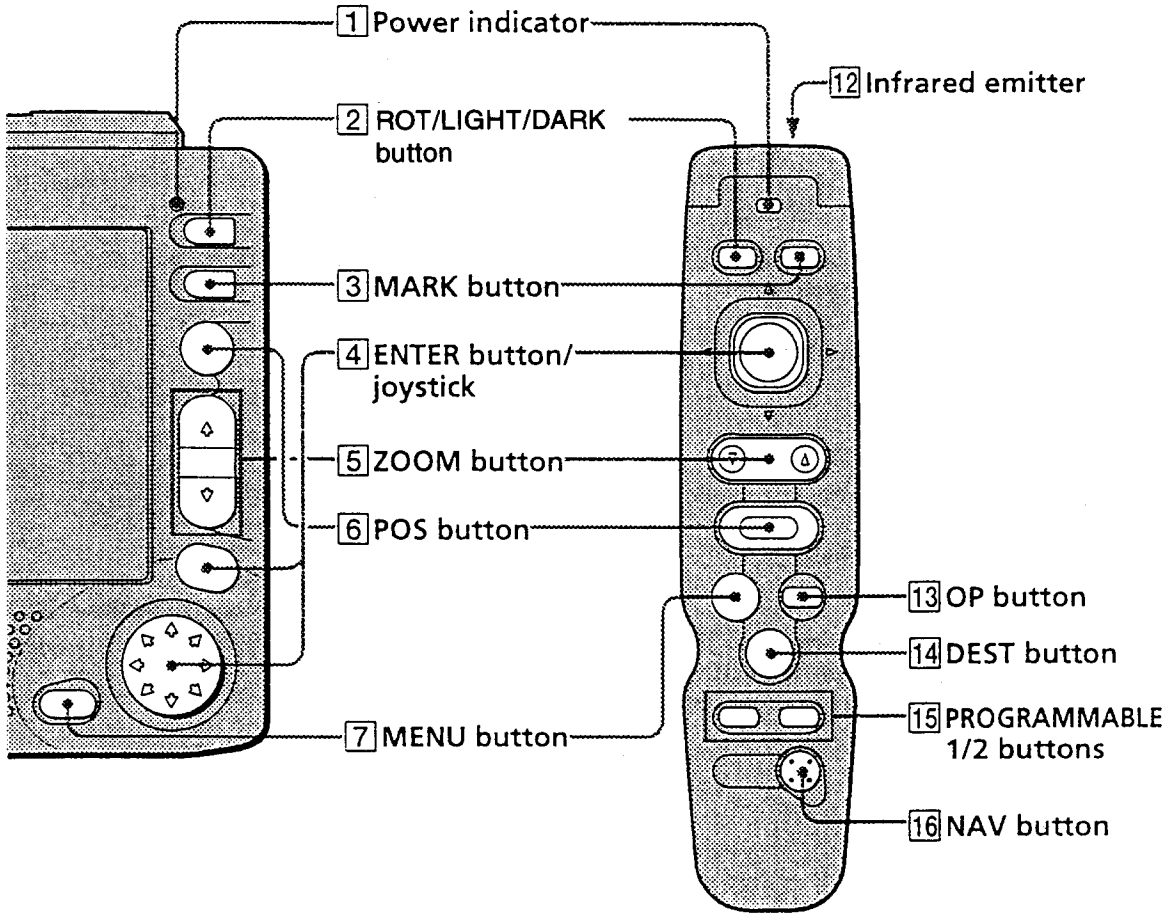
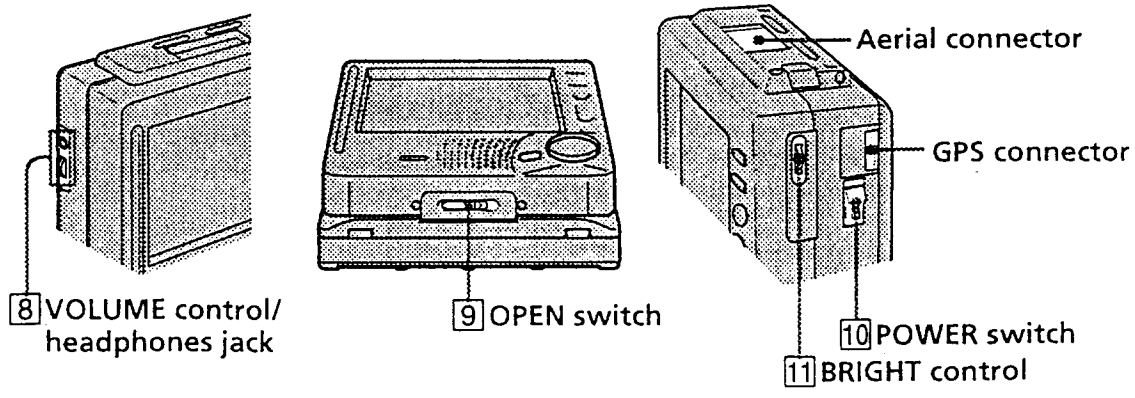
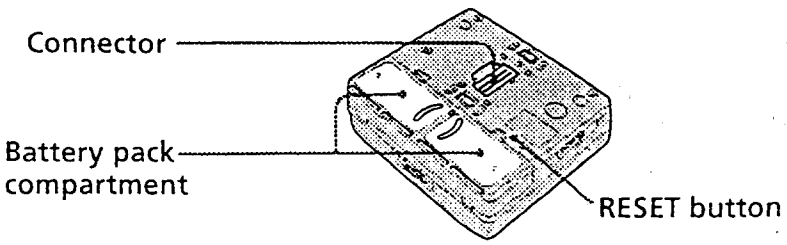
This section extracted from instruction manual.

Location and Function of Controls







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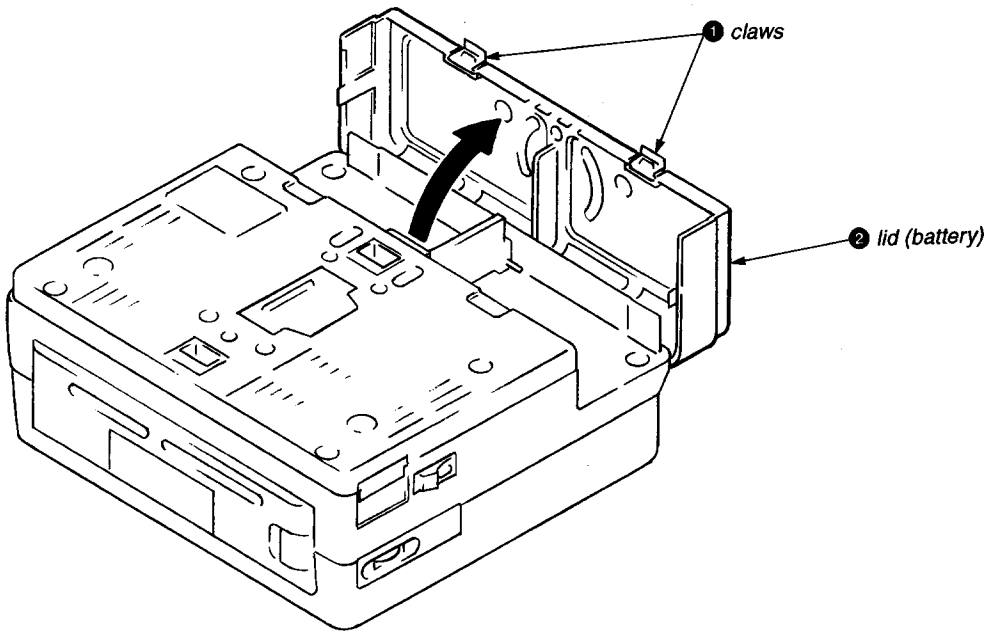
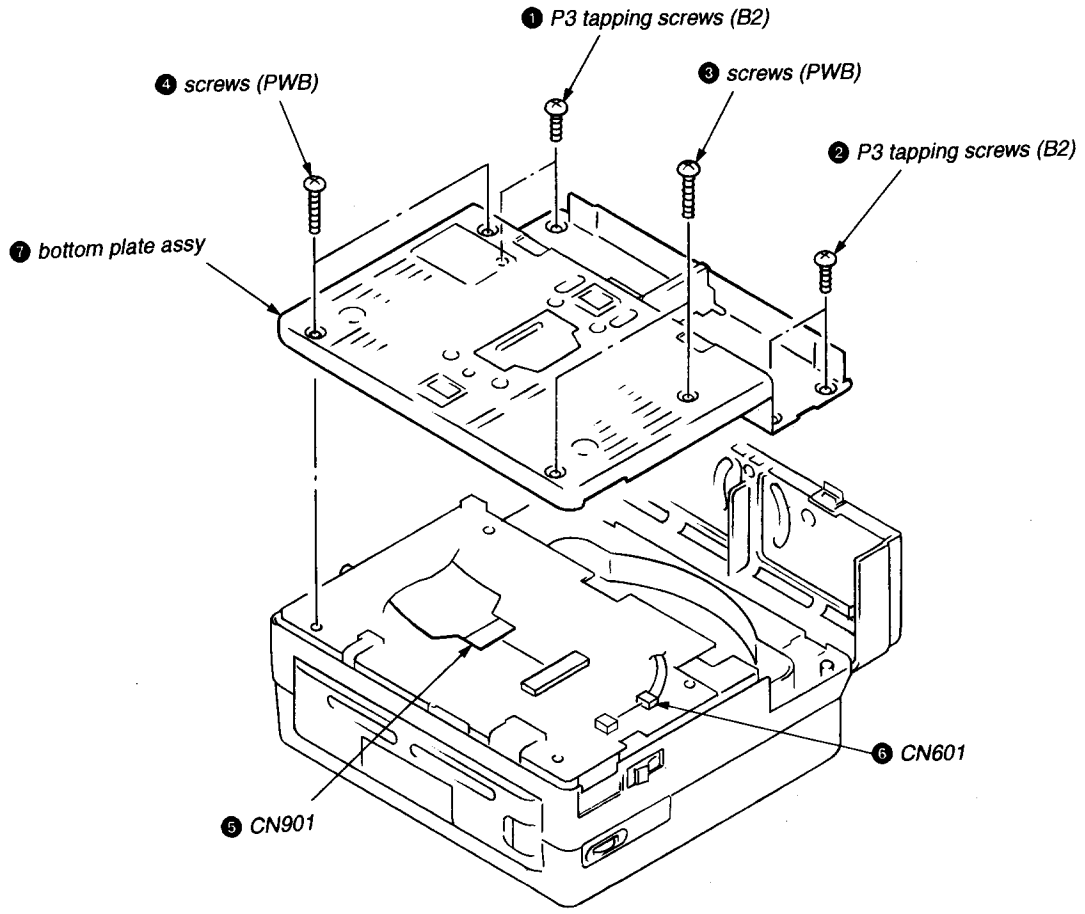
SECTION 2
DISASSEMBLY

Note : Follow the disassembly procedure in the numerical order givin.

2-1. LID (BATTERY)

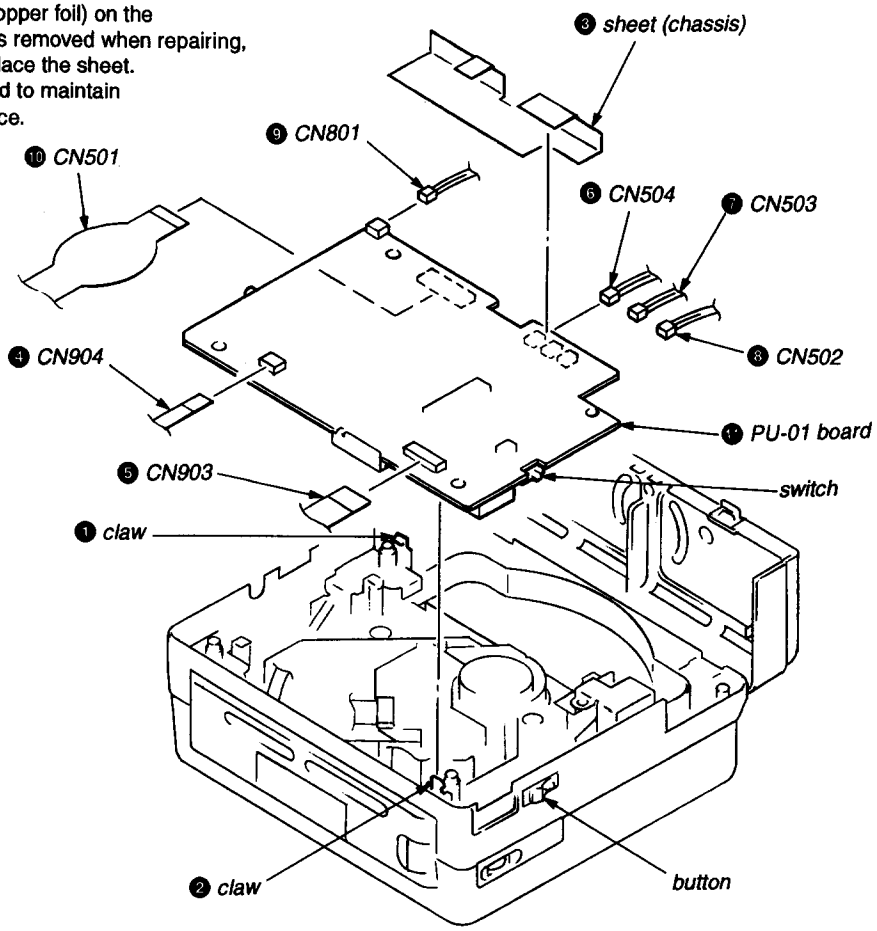


2-2. BOTTOM PLATE ASSY

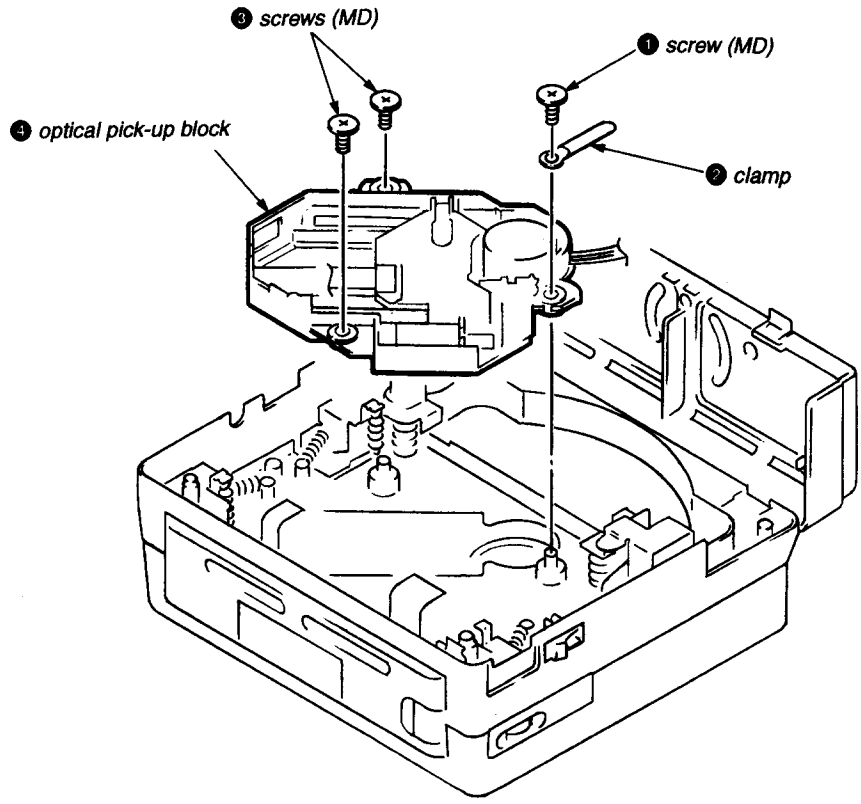


2-3. PU-01 BOARD

Note : When installing, fit the position the switch and button.
If the sheet (copper foil) on the PU-01 board is removed when repairing, be sure to replace the sheet.
This is required to maintain the performance.

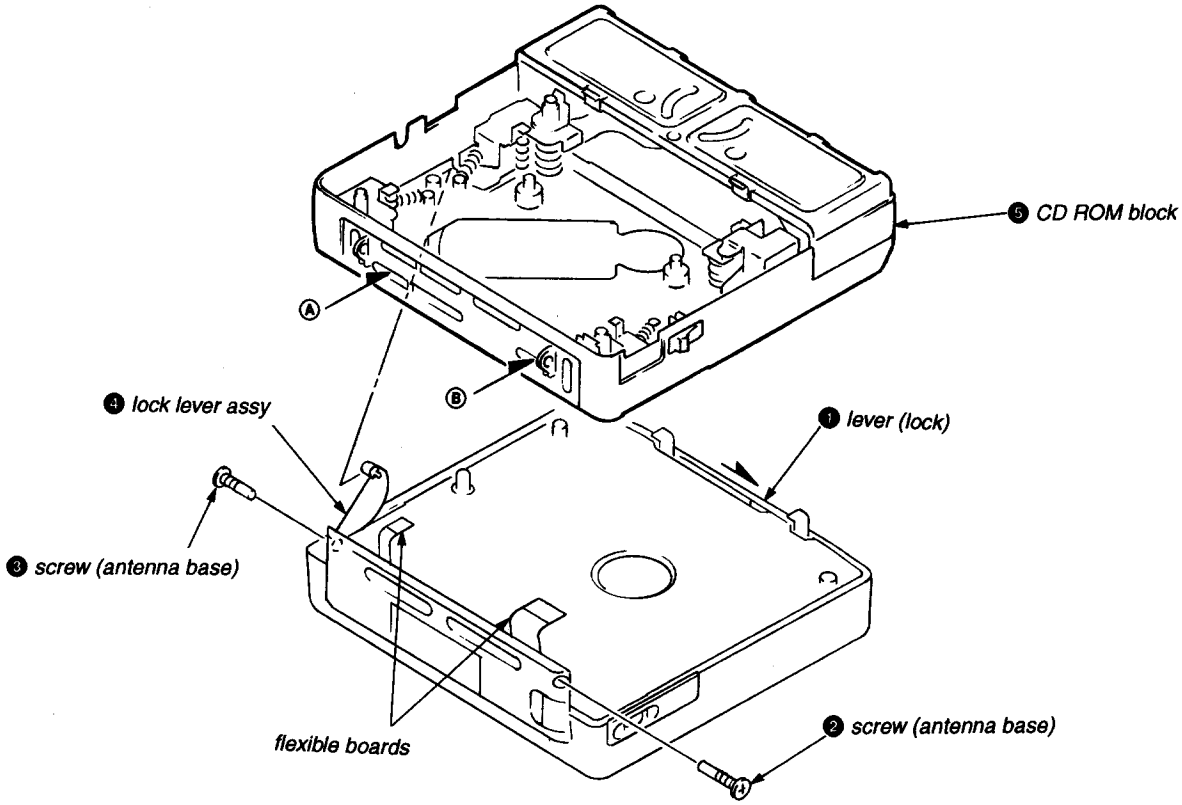


2-4. OPTICAL PICK-UP BLOCK

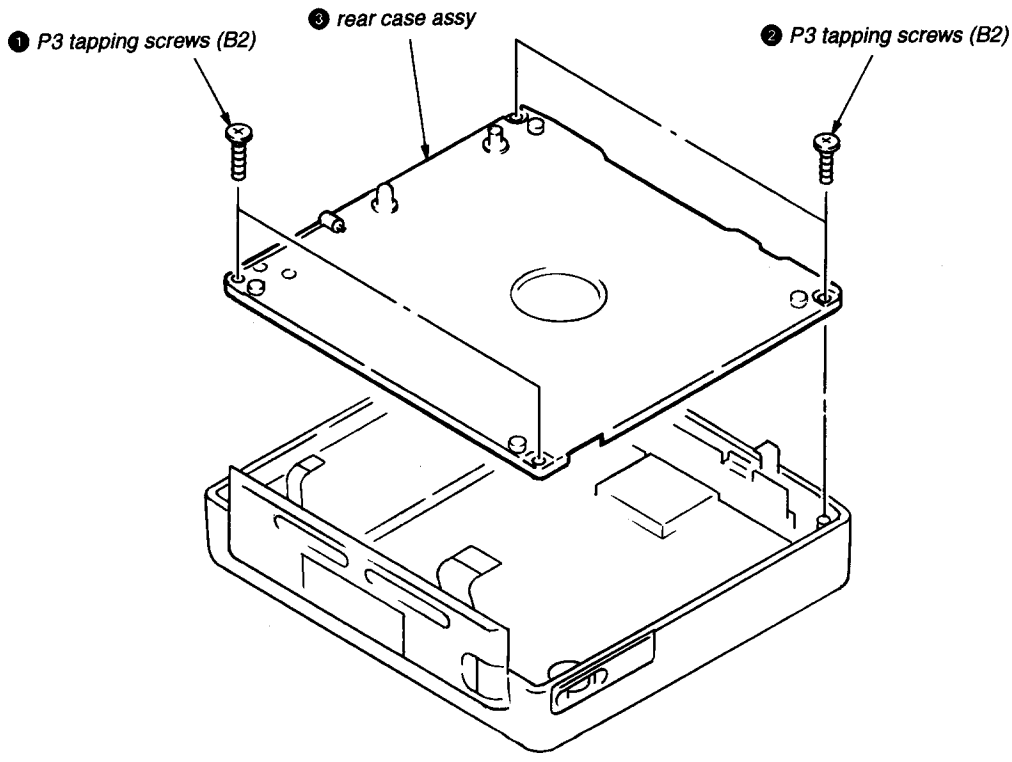


2-5. CD ROM BLOCK

Note : When installing, through the flexible board in holes Ⓐ and Ⓑ.

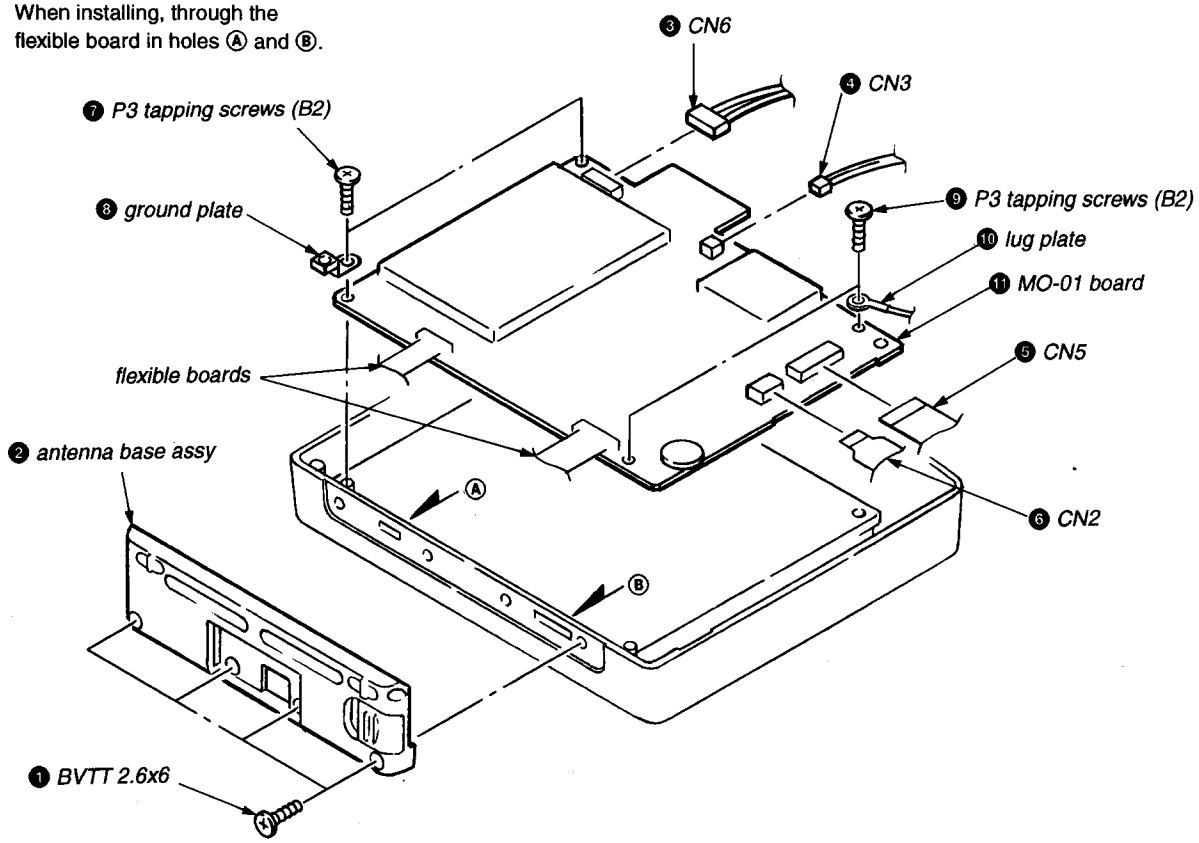


2-6. REAR CASE ASSY

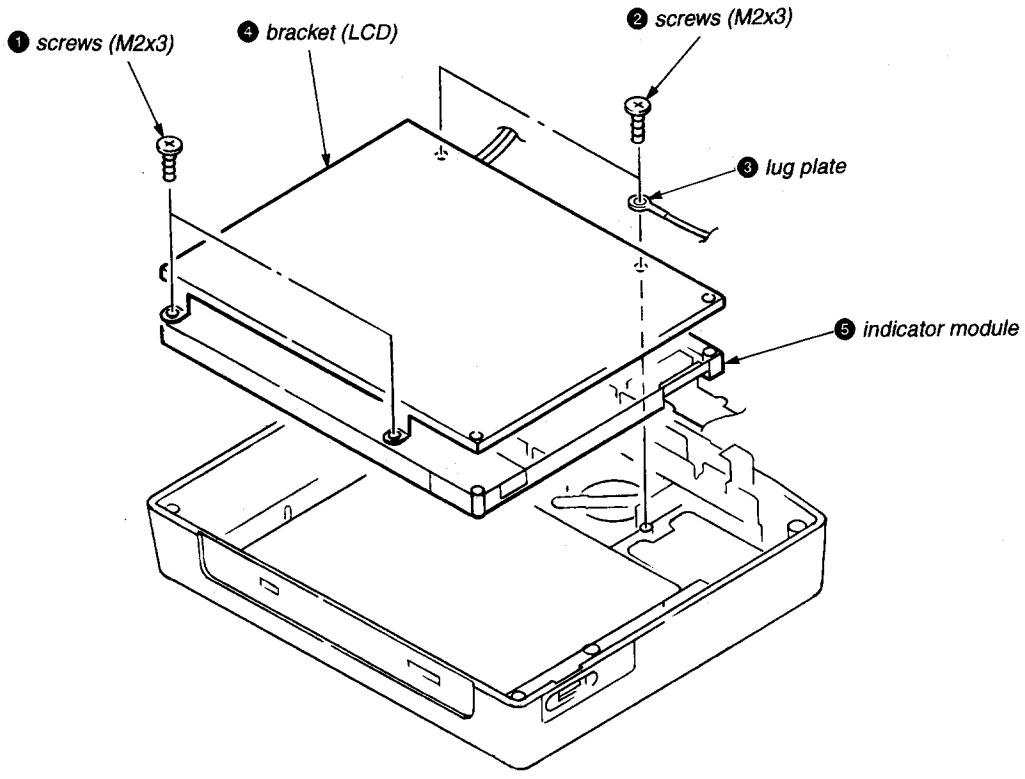


2-7. MO-01 BOARD

Note : When installing, through the flexible board in holes Ⓐ and Ⓑ.



2-8. INDICATOR MODULE



SECTION 3
ELECTRICAL ADJUSTMENTS

CD ROM SECTION

Notes on Adjustments

1. Perform adjustments in the order given.
2. Use the disc (YEDS-18, Part No. 3-702-101-01) only when so indicated.

D5V Adjustment

Procedure :

1. Connect a digital voltmeter to the test point TP601 on the PU-01 board.
2. Turn on the POWER.
3. Adjust RV601 so that reading on the digital voltmeter becomes 5.0 ± 0.1 V.

Adjustment Location : See page 10.

A5V Adjustment

Procedure :

1. Connect a digital voltmeter to the test point TP602 on the PU-01 board.
2. Turn on the POWER.
3. Adjust RV602 so that reading on the digital voltmeter becomes 5.0 ± 0.1 V.

Adjustment Location : See page 10.

Trimmer Adjustment

Procedure :

1. Connect a digital frequency counter to the test point TP715 on the PU-01 board.
2. Turn on the POWER.
3. Adjust CT701 so that reading on the digital frequency counter becomes 3.5795 to 3.5796 MHz.

Adjustment Location : See page 10.

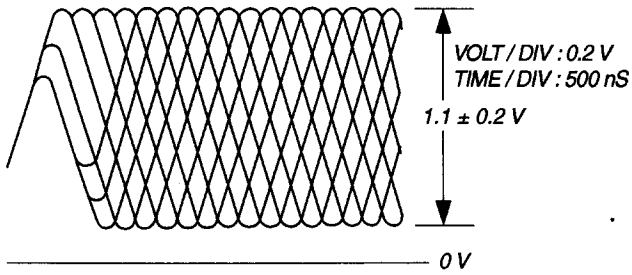
Focus Bias Adjustment

Setting : This adjustment is performed with the set at level.

Procedure :

1. Connect an oscilloscope between the test points TP501 (RF) and TP504 (VC) on the PU-01 board.
2. Set the disc (YEDS-18) and close the upper lid.
3. Turn on the POWER.
4. Adjust RV501 so that the rhomboid is clearly discriminated in the center of the eye pattern waveform on the oscilloscope.

• RF signal reference waveform (eye pattern)

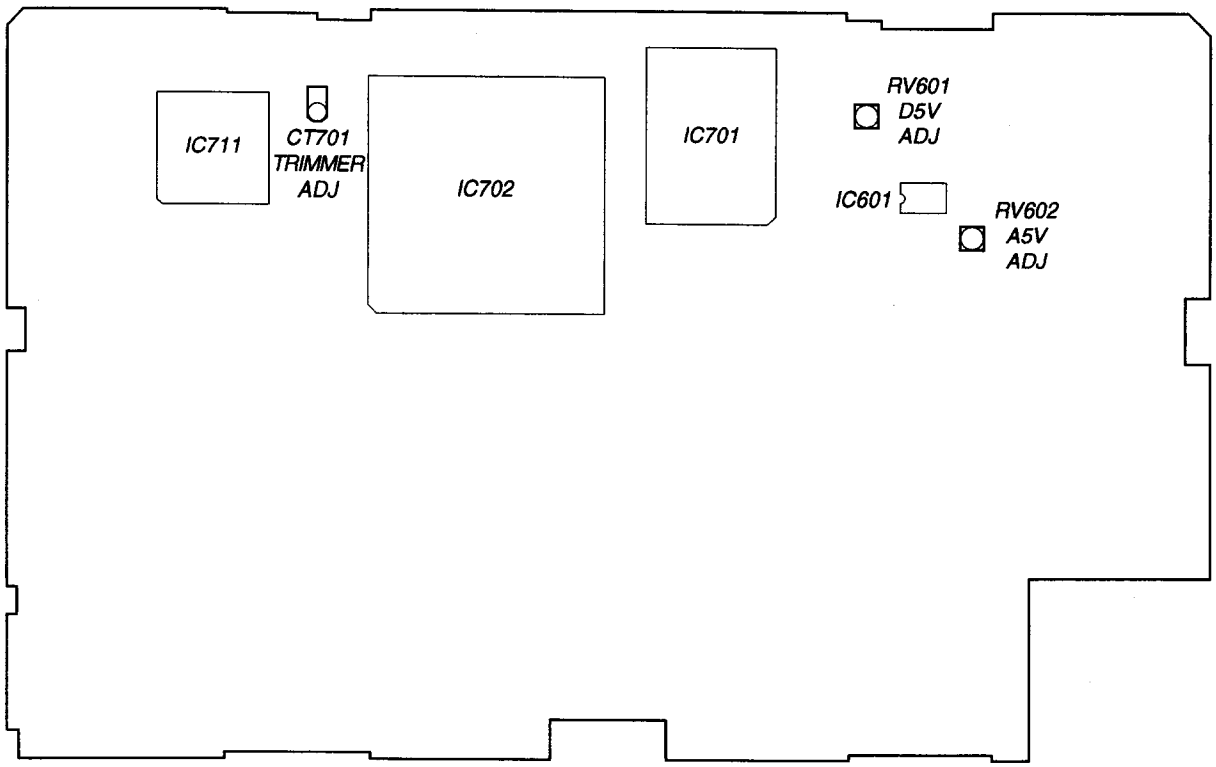


When observing the eye pattern, set the oscilloscope for AC range and raise vertical sensitivity.

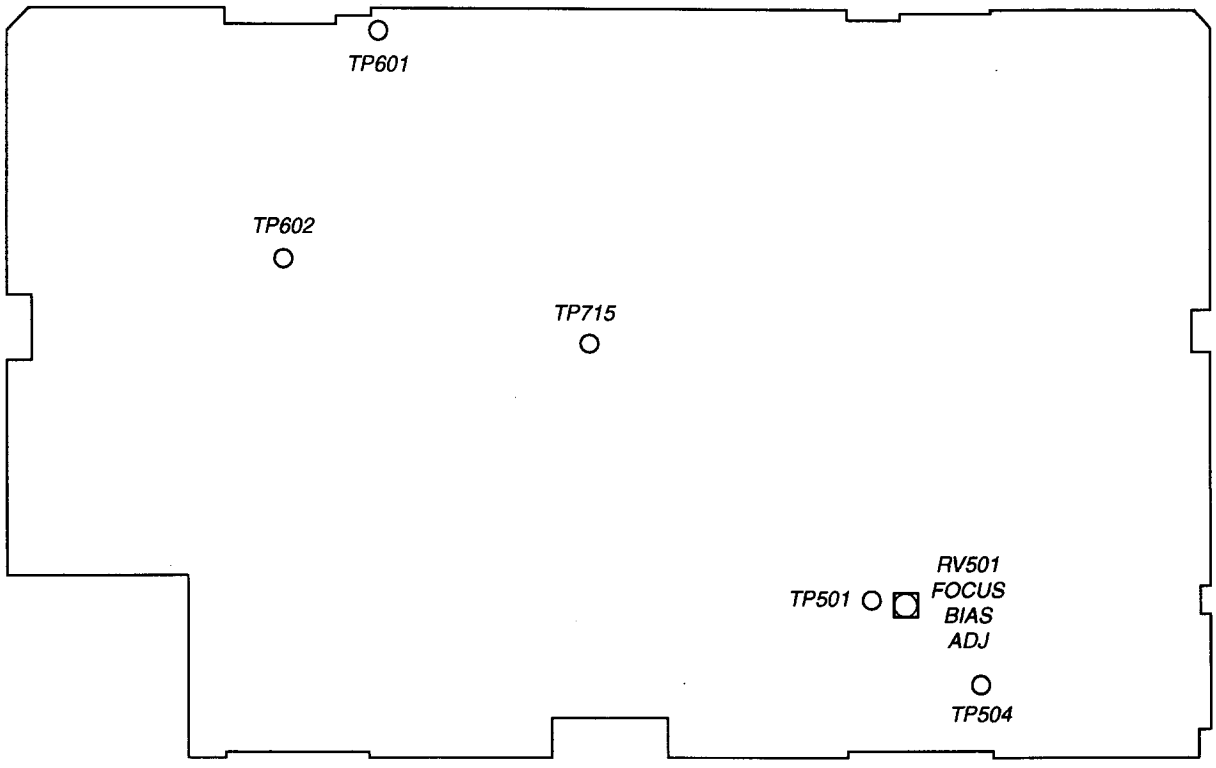
Adjustment Location : See page 10.

Adjustment Location :

– PU-01 board (side A) –



– PU-01 board (side B) –



MONITOR SECTION

Note: V • BIAS adjustment should be always carried out when the indicator module (LCD901) is replaced.

Setting the Test Mode

1. Turn on the POWER. When the menu screen is displayed, press the ZOOM buttons in the following order : △ → ▽ → △ → ▽ → MARK button.
2. The Test Mode menu appears on the monitor.
3. Use the joystick to move the cursor to the COLOR CHECK, then press the ENTER button.
4. The color bar appears on the monitor.
5. Push the joystick to the left (◁) once to display the gray scale. Repeatedly push the joystick to change the monitor from one to another.

Releasing the Test Mode

1. Turn off the POWER.

Equipment Used

The following measuring equipment are used to adjust the monitor section.

- Oscilloscope dual, 10 MHz or more bandwidth, with delay mode. (Unless otherwise specified, 10 : 1 probe should be used.)

Power Voltage Adjustment

Procedure :

1. Connect a digital voltmeter to the test point CL30 on the MO-01 board.
2. Turn on the POWER.
3. Adjust RV14 (12.8V) so that reading on the digital voltmeter becomes 12.8 ± 0.1 V.

Adjustment Location : See page 13.

V • BIAS Adjustment

Procedure :

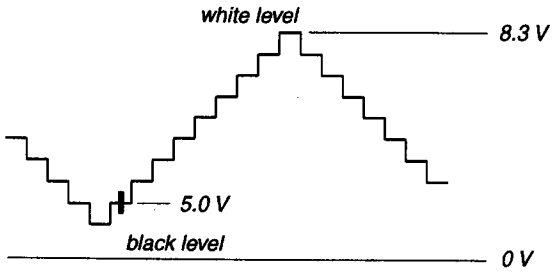
1. Remove solder bridge at the test point SL1A on the MO-01 board.
2. Connect an ammeter between the test points CL76 (+) and CL38 (–) on the MO-01 board.
3. Turn on the POWER.
4. Adjust RV15 (V • BIAS) so that reading on the ammeter becomes 26 ± 1 mA.
5. After this adjustment, solder bridge the test point SL1A.

Adjustment Location : See page 13.

White Balance Adjustment

Procedure :

1. Set the test mode, to display gray scale on the monitor.
2. Set the BRIGHT control (RV7) in the mechanical center.
3. Connect an oscilloscope to the test point CL40 on the MO-01 board.
4. Adjust RV12 (G SUB BRIT) so that the lower black level is at 5.0 ± 0.1 V.
5. Adjust RV2 (VI CONT) so that the upper 100% white level is at 8.3 ± 0.1 V.
6. Repeat items 4 and 5 until the specification is met.
7. Connect an oscilloscope to the test point CL42 on the MO-01 board.
8. Adjust RV11 (R SUB BRIT) so that the lower black level is at 5.0 ± 0.1 V.
9. Adjust RV5 (R CONT) so that the upper 100% white level is at 8.3 ± 0.1 V.
10. Repeat items 8 and 9 until the specification is met.
11. Connect an oscilloscope to the test point CL41 on the MO-01 board.
12. Adjust RV13 (B SUB BRIT) so that the lower black level is at 5.0 ± 0.1 V.
13. Adjust RV3 (B CONT) so that the upper 100% white level is at 8.3 ± 0.1 V.
14. Repeat items 12 and 13 until the specification is met.



Adjustment Location : See page 13.

PLL Adjustment

Procedure :

1. Connect a digital voltmeter to the test point CL36 on the MO-01 board.
2. Turn on the POWER.
3. Adjust LV1 (PLL) so that reading on the digital voltmeter becomes 2.5 ± 0.2 V.

Adjustment Location : See page 13.

V COM Adjustment

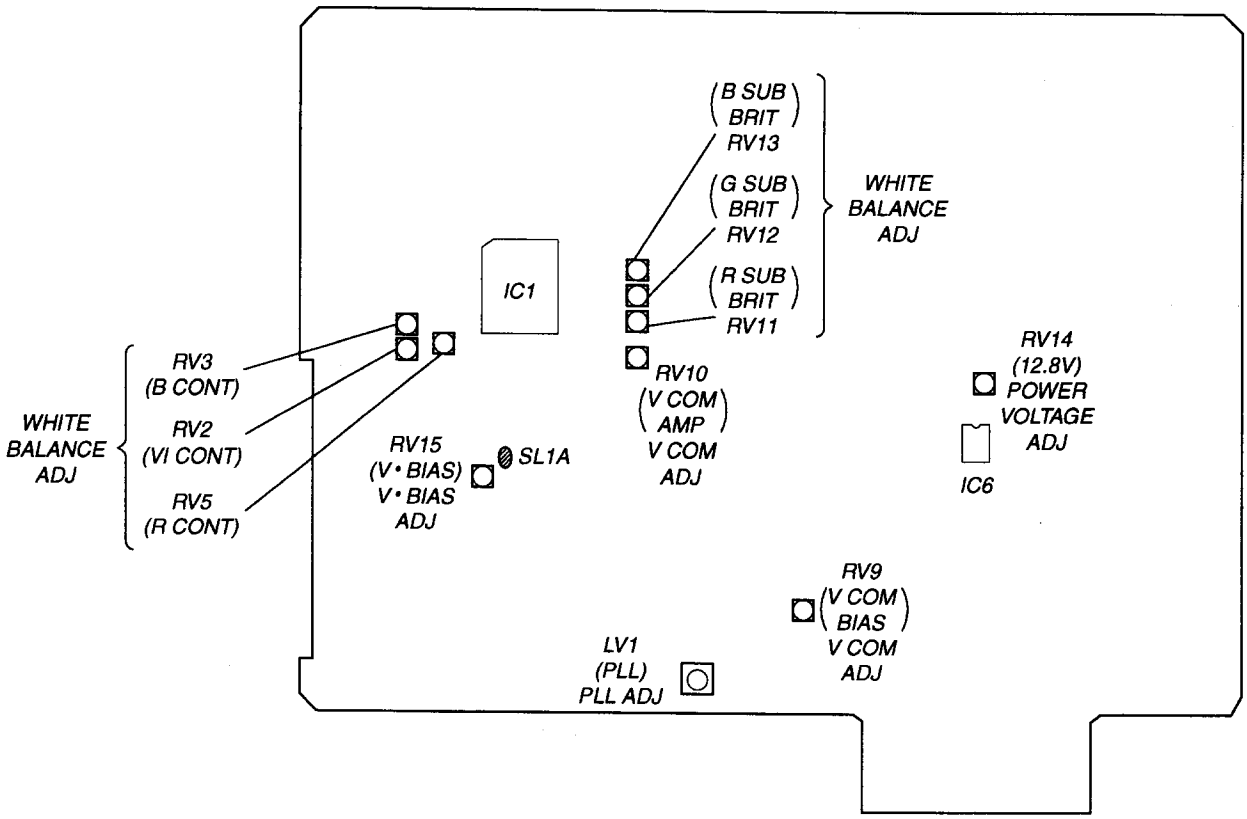
Procedure :

1. Set the test mode (see page 11.), to display gray scale on the monitor.
2. Set the BRIGHT control (RV7) in the mechanical center.
3. Observe the monitor screen and adjust RV9 (V COM BIAS) so that the contrast is maximized.
4. Adjust RV10 (V COM AMP) so that the gray scale is balanced in upset between white and black sides.

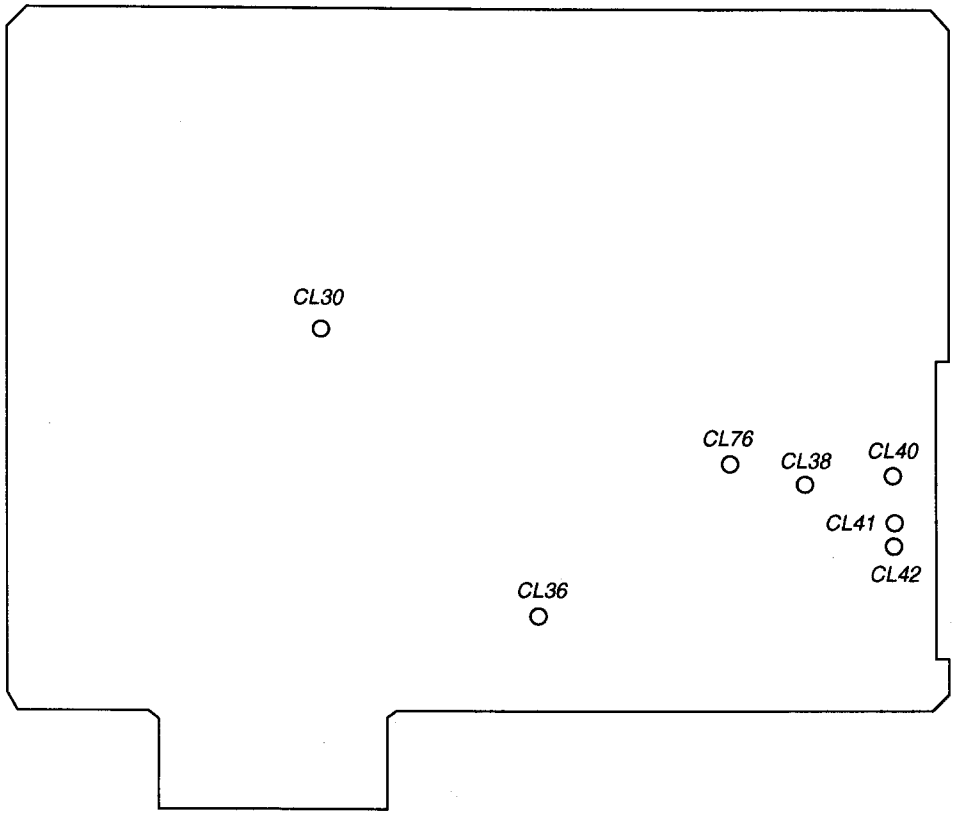
Adjustment Location : See page 13.

Adjustment Location :

– MO-01 board (side A) –



– MO-01 board (side B) –



SECTION 4
DIAGRAMS

4-1. IC PIN DESCRIPTIONS

• IC701 MC68EC020FG-16 (CPU)

Pin No.	Pin Name	I/O	Pin Description
1	$\overline{BR}$	I	Bus request input for CPU data bus line.
2	$\overline{BG}$	O	Bus ground output for CPU data bus line.
3, 4	GND	—	GND
5	CLK	I	Clock input from CD ROM AV control (IC702 CXD2928AQ).
6	$\overline{RESET}$	I/O	System reset signal input ("L" : Reset)
7, 8	VCC	—	Power supply (+5 V)
9	$\overline{RMC}$	—	Not used.
10 – 12	FC0 – FC2	—	Not used.
13	SIZ0	O	Data size appointment output 0 for CPU data bus line.
14	SIZ1	O	Data size appointment output 1 for CPU data bus line.
15	$\overline{CDIS}$	—	Not used.
16	$\overline{AVEC}$	—	Fixed at "H" in this set.
17	$\overline{DSACK0}$	I	Data acknowledge input 0 for CPU data bus line.
18	$\overline{DSACK1}$	I	Data acknowledge input 1 for CPU data bus line.
19	$\overline{BERR}$	—	Fixed at "H" in this set.
20, 21	GND	—	GND
22	$\overline{HALT}$	I	System reset signal input
23	$\overline{AS}$	O	Address strobe output for CPU data bus line.
24	$\overline{DS}$	O	Data strobe output for CPU data bus line.
25	R/$\overline{W}$	O	Read/Write select output for CPU data bus line.
26	GND	—	GND
27	D31	I/O	Data input/output for CPU data bus line. (D31)
28	D30	I/O	Data input/output for CPU data bus line. (D30)
29	D29	I/O	Data input/output for CPU data bus line. (D29)
30	D28	I/O	Data input/output for CPU data bus line. (D28)
31	D27	I/O	Data input/output for CPU data bus line. (D27)
32	D26	I/O	Data input/output for CPU data bus line. (D26)
33	D25	I/O	Data input/output for CPU data bus line. (D25)
34	D24	I/O	Data input/output for CPU data bus line. (D24)
35	D23	I/O	Data input/output for CPU data bus line. (D23)
36	D22	I/O	Data input/output for CPU data bus line. (D22)
37	D21	I/O	Data input/output for CPU data bus line. (D21)
38	D20	I/O	Data input/output for CPU data bus line. (D20)
39	D19	I/O	Data input/output for CPU data bus line. (D19)
40	D18	I/O	Data input/output for CPU data bus line. (D18)
41	D17	I/O	Data input/output for CPU data bus line. (D17)
42	D16	I/O	Data input/output for CPU data bus line. (D16)
43	GND	—	GND
44	VCC	—	Power supply (+5 V)
45	D15	I/O	Data input/output for CPU data bus line. (D15)
46	D14	I/O	Data input/output for CPU data bus line. (D14)
47	D13	I/O	Data input/output for CPU data bus line. (D13)
48	D12	I/O	Data input/output for CPU data bus line. (D12)
49	D11	I/O	Data input/output for CPU data bus line. (D11)
50	D10	I/O	Data input/output for CPU data bus line. (D10)
51	D9	I/O	Data input/output for CPU data bus line. (D9)
52	NC	—	Not used.

Pin No.	Pin Name	I/O	Pin Description
53	D8	I/O	Data input/output for CPU data bus line. (D8)
54	D7	I/O	Data input/output for CPU data bus line. (D7)
55	D6	I/O	Data input/output for CPU data bus line. (D6)
56	D5	I/O	Data input/output for CPU data bus line. (D5)
57	VCC	—	Power supply (+5 V)
58, 59	GND	—	GND
60	D4	I/O	Data input/output for CPU data bus line. (D4)
61	D3	I/O	Data input/output for CPU data bus line. (D3)
62	D2	I/O	Data input/output for CPU data bus line. (D2)
63	D1	I/O	Data input/output for CPU data bus line. (D1)
64	D0	I/O	Data input/output for CPU data bus line. (D0)
65	$\overline{\text{IPL0}}$	—	Fixed at "H" in this set.
66	$\overline{\text{IPL1}}$	I	Interrupt request input from CD ROM AV control (IC702 CXD2928AQ). At request : "L", at non-request : "H"
67	$\overline{\text{IPL2}}$	—	Fixed at "H" in this set.
68, 69	GND	—	GND
70, 71	VCC	—	Power supply (+5 V)
72	GND	—	GND
73	A2	O	Address output for CPU address bus line. (A2)
74	A3	O	Address output for CPU address bus line. (A3)
75	A4	O	Address output for CPU address bus line. (A4)
76	A5	O	Address output for CPU address bus line. (A5)
77	A6	O	Address output for CPU address bus line. (A6)
78	A7	O	Address output for CPU address bus line. (A7)
79	NC	—	Empty pin
80	A8	O	Address output for CPU address bus line. (A8)
81	A9	O	Address output for CPU address bus line. (A9)
82	A10	O	Address output for CPU address bus line. (A10)
83	A11	O	Address output for CPU address bus line. (A11)
84	A12	O	Address output for CPU address bus line. (A12)
85	A13	O	Address output for CPU address bus line. (A13)
86	A14	O	Address output for CPU address bus line. (A14)
87	A15	O	Address output for CPU address bus line. (A15)
88	A16	O	Address output for CPU address bus line. (A16)
89	GND	—	GND
90	VCC	—	Power supply (+5 V)
91	A17	O	Address output for CPU address bus line. (A17)
92	A18	O	Address output for CPU address bus line. (A18)
93	A19	O	Address output for CPU address bus line. (A19)
94	A20	O	Address output for CPU address bus line. (A20)
95	A21	O	Address output for CPU address bus line. (A21)
96	A22	O	Address output for CPU address bus line. (A22)
97	A23	O	Address output for CPU address bus line. (A23)
98	A1	O	Address output for CPU address bus line. (A1)
99	A0	O	Address output for CPU address bus line. (A0)
100	GND	—	GND

• **IC702 CXD2928AQ (CD ROM AV CONTROL)**

Pin No.	Pin Name	I/O	Pin Description
1	VSS	—	GND
2	GCK	O	Video clock output (3.58 MHz)
3	EXT	I	External superimpose input enable signal (Negative logic). (Not used in this set.)
4	ADC	O	Clock for A/D change. (Not used in this set.)
5	VTS	I	Mode setting (Fixed at "H" in this set.)
6	XOT	O	Crystal oscillator output (Not used in this set.)
7	XIN	I	Crystal oscillator input
8 – 19	S15 – S04	I	Picture data input (MSB : S15)
20	VDD	—	Power supply (+5 V)
21 – 24	S03 – S00	I	Picture data input (LSB : S00)
25	SC0	O	Serial clock output for VRAM.
26	SE2	O	Serial port enable output for VRAM. (Not used in this set.)
27	SE1	O	Serial port enable output for VRAM.
28	PBDT	O	DT/OE output for VRAM.
29	PBWB	O	WE output for VRAM.
30, 31	PBR3, PBR2	O	RAS output for DRAM.
32	PBR1	O	RAS output for VRAM. (For D24 to D31 chip.)
33	PBR0	O	RAS output for VRAM. (For D16 to D23 chip.)
34	PRA8	O	Address output for VRAM. (A8)
35	PRA7	O	Address output for VRAM. (A7)
36	PRA6	O	Address output for VRAM. (A6)
37	PRA5	O	Address output for VRAM. (A5)
38	PRA4	O	Address output for VRAM. (A4)
39	PRA3	O	Address output for VRAM. (A3)
40	VDD	—	Power supply (+5 V)
41	VSS	—	GND
42	PRA2	O	Address output for VRAM. (A2)
43	PRA1	O	Address output for VRAM. (A1)
44	PRA0	O	Address output for VRAM. (A0)
45	PBC3	O	CAS output for VRAM. (For chip allocated to lower 512 kbyte at D16 to D23.)
46	PBC2	O	CAS output for VRAM. (For chip allocated to lower 512 kbyte at D24 to D31.)
47	PBC1	O	CAS output for VRAM. (For chip allocated to upper 512 kbyte at D16 to D23.)
48	PBC0	O	CAS output for VRAM. (For chip allocated to upper 512 kbyte at D24 to D31.)
49	PXAE	O	E00000 address decode output (Automatic generation of gated DTACK at /AS.)
50	PXAD	O	D00000 address decode output (Automatic generation of gated DTACK at /AS.)
51	PXAC	O	C00000 address decode output (Automatic generation of gated DTACK at /AS.) (Not used in this set.)
52	VSS	—	GND
53	PCSX	O	Empty area chip select signal (1FFFFF to AFFFFF) (No generation of gated DTACK at /AS.)
54	PXRO	O	Boot ROM chip select signal (Automatic generation of 000000 to 000006 or F00000 to FFFFFF DTACK.)
55	VSS	—	GND
56	PA1	I/O	Address input from/output for CPU BUS. (A1)
57	PA2	I/O	Address input from/output for CPU BUS. (A2)
58	PA3	I/O	Address input from/output for CPU BUS. (A3)
59	VSS	—	GND

Pin No.	Pin Name	I/O	Pin Description
60	PA4	I/O	Address input from/output for CPU BUS. (A4)
61	PA5	I/O	Address input from/output for CPU BUS. (A5)
62	PA6	I/O	Address input from/output for CPU BUS. (A6)
63	PA7	I/O	Address input from/output for CPU BUS. (A7)
64	PA8	I/O	Address input from/output for CPU BUS. (A8)
65	PA9	I/O	Address input from/output for CPU BUS. (A9)
66	PA10	I/O	Address input from/output for CPU BUS. (A10)
67	PA11	I/O	Address input from/output for CPU BUS. (A11)
68	PA12	I/O	Address input from/output for CPU BUS. (A12)
69	PA13	I/O	Address input from/output for CPU BUS. (A13)
70	PA14	I/O	Address input from/output for CPU BUS. (A14)
71	PA15	I/O	Address input from/output for CPU BUS. (A15)
72	PA16	I/O	Address input from/output for CPU BUS. (A16)
73	PA17	I/O	Address input from/output for CPU BUS. (A17)
74	PA18	I/O	Address input from/output for CPU BUS. (A18)
75	PA19	I/O	Address input from/output for CPU BUS. (A19)
76	PA20	I/O	Address input from/output for CPU BUS. (A20)
77	PA21	I/O	Address input from/output for CPU BUS. (A21)
78	PA22	I/O	Address input from/output for CPU BUS. (A22)
79	PA23	I/O	Address input from/output for CPU BUS. (A23)
80	VDD	—	Power supply (+5 V)
81	VSS	—	GND
82	PD15	I/O	Data input from/output for CPU BUS. (D31)
83	PD14	I/O	Data input from/output for CPU BUS. (D30)
84	PD13	I/O	Data input from/output for CPU BUS. (D29)
85	PD12	I/O	Data input from/output for CPU BUS. (D28)
86	PD11	I/O	Data input from/output for CPU BUS. (D27)
87	PD10	I/O	Data input from/output for CPU BUS. (D26)
88	PD9	I/O	Data input from/output for CPU BUS. (D25)
89	PD8	I/O	Data input from/output for CPU BUS. (D24)
90	PD7	I/O	Data input from/output for CPU BUS. (D23)
91	PD6	I/O	Data input from/output for CPU BUS. (D22)
92	PD5	I/O	Data input from/output for CPU BUS. (D21)
93	PD4	I/O	Data input from/output for CPU BUS. (D20)
94	PD3	I/O	Data input from/output for CPU BUS. (D19)
95	PD2	I/O	Data input from/output for CPU BUS. (D18)
96	PD1	I/O	Data input from/output for CPU BUS. (D17)
97	PD0	I/O	Data input from/output for CPU BUS. (D16)
98	PXNB	O	B00000 address decode output (Automatic generation of DTACK not gated at /AS.)
99	PXAS	I/O	Address strobe input from/output for CPU BUS.
100	PXUS	I/O	Data strobe input from/output for CPU BUS. (DS)
101	PXLS	I/O	Address input from/output for CPU BUS. (A0)
102	PRW	I/O	Read/Write input from/output for CPU BUS.
103	PXDK	I/O	Data acknowledge input from/output for CPU BUS. (DSACK1)
104	PXBG	I	Bus grant input from CPU BUS.
105	PXBK	O	Bus grant acknowledge output for CPU BUS.
106	PXBR	O	Bus request output for CPU BUS.

Pin No.	Pin Name	I/O	Pin Description
107	PXIR	O	Interrupt request output for CPU. (At request : "L", at no request : High impedance)
108	PXRS	I	Reset input ("L" : Reset)
109	VSS	—	GND
110	PIO0	I/O	General-purpose I/O port bit 0 (SIZE 0)
111	PIO1	I/O	General-purpose I/O port bit 1 (SIZE 1)
112	PIO2	I/O	General-purpose I/O port bit 2 (DSACK 0)
113	PIO3	I/O	General-purpose I/O port bit 3
114	PXRA	I	Request input from CXD8554R (Sound Chip). ("L" : With request)
115	PINH	I	Mode setting (Fixed at "H" in this set.)
116	PCCK	O	Clock output for CPU. (=1/2MCK)
117	PMCK	O	Master clock output (MCK)
118	TEST1	I	Test pin 1
119	TEST0	I	Test pin 2
120	VDD	—	Power supply (+5 V)
121	VSS	—	GND
122	XOT2	O	Crystal connecting pin output for master clock oscillator (28.63636 MHz)
123	XIN2	I	Crystal connecting pin input for master clock oscillator (28.63636 MHz)
124	PTXD	O	ACIA CH1 data output
125	PRXD	I	ACIA CH1 data input
126	PMDT	O	Command output to CD-ROM drive.
127	PMST	I	Status input from CD-ROM drive.
128	PC2P	I	C2 flag input from CD-ROM drive.
129	PDAT	I	Data input from CD-ROM drive.
130	PLCK	I	Data LR CLOCK input from CD-ROM drive.
131	PBCK	I	Data BIT CLOCK input from CD-ROM drive.
132	PTX2	O	ACIA CH2 data output
133	PRX2	I	ACIA CH2 data input
134	PTX3	O	ACIA CH3 data output
135	PRX3	I	ACIA CH3 data input
136	PSIN	I	External composite sync input (Fixed at "L" in this set.)
137	PCSC	O	Composite sync output
138	PHSC	O	H SYNC signal output (Not used in this set.)
139	PHBK	O	Write enable output for program ROM.
140	PVSC	O	V BLANK signal output (Not used in this set.)
141	PVBK	O	Output enable output for program ROM.
142	PIO4	I/O	General-purpose I/O port bit 4
143	PIO5	I/O	General-purpose I/O port bit 5
144	PIO6	I/O	General-purpose I/O port bit 6
145	PIO7	I/O	General-purpose I/O port bit 7
146	PIO8	I/O	General-purpose I/O port bit 8
147	PIO9	I/O	General-purpose I/O port bit 9
148	PIOA	I/O	General-purpose I/O port bit A
149	AVSS	—	Analog GND
150	PIOB	I/O	General-purpose I/O port bit B
151	MUTE	I	Video signal mute ("H" : OUT = 0 V and PCSC = 5 V, "L" : Normally output)
152	VB	I	Bias voltage generation
153	AVSS	—	Analog GND

Pin No.	Pin Name	I/O	Pin Description
154	VREF	—	V reference (Setting of output full scale value.)
155	IREF	—	I reference
156	ROUT	O	Red current output terminal
157	GOUT	O	Green current output terminal
158	BOUT	O	Blue current output terminal
159	VG	I	Current cell
160	VDD	—	Power supply (+5 V)

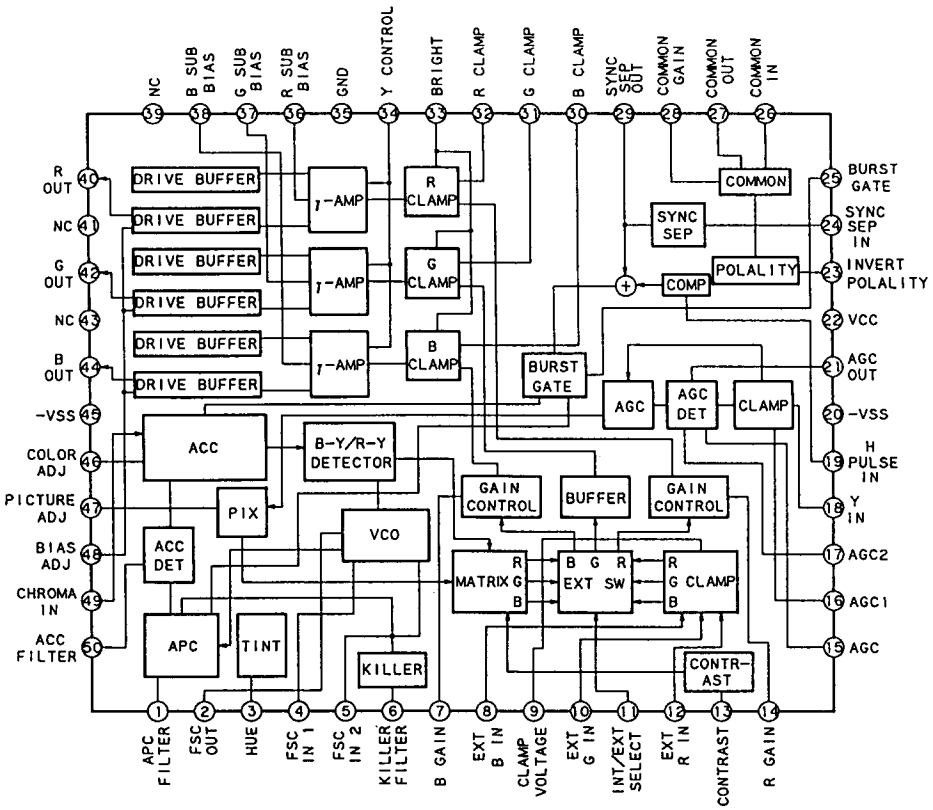
• IC801 μPD78054GC-189-3B9 (CD MICRO COMPUTER)

Pin No.	Pin Name	I/O	Pin Description
1	$\overline{\text{SIDBRK}}$	I	Side brake mode input of a car. ("L" : Side brake (Parking brake) ON)
2	AMPREM	O	Amplifier remote control output ("H" : Amplifier remote ON) (Not used in this set.)
3	PWLED	O	System ON/OFF mode LED indicator output
4	AVSS	—	A/D converter GND
5	MDATA	I	Serial data input and serial clock input from CXD2928AQ (IC702).
6	MSTAT	O	Serial data output and serial clock output for CXD2928AQ (IC702).
7	AVREF1	—	D/A converter reference voltage
8	MRX	I	Communication data input for system control monitor. (Not used in this set.)
9	MTX	O	Communication data output for system control monitor. (Not used in this set.)
10	$\overline{\text{TEST1}}$	I	Test mode 1 setting switch input
11	SUBQ	I	Sub code Q data serial data input
12	P21/S01	O	Not used.
13	SQCK	O	Sub code Q data serial clock output
14	P23	O	Loading motor control output (Eject direction) (Not used in this set.)
15	P24	O	Loading motor control output (Loading direction) (Not used in this set.)
16	$\overline{\text{TEST2}}$	I	Test mode 2 setting switch input
17	XDATA	O	Digital servo IC control serial data output
18	XCLK	O	Digital servo IC control serial clock output
19	GFS	I	Frame sync lock mode input
20	SENS	I	SENS data input from digital servo IC.
21	FOK	I	Focus OK input ("H" : Focus OK)
22	$\overline{\text{DUBSEL}}$	I	CD-ROM double-speed PLAY function select switch input ("L" : CD-ROM double-speed select)
23	$\overline{\text{MOVSEL}}$	I	Operation sensor function select ("L" : With operation sensor function)
24	GPSANT	I	GPS connect
25	$\overline{\text{STATION}}$	I	Car station/Home station connect signal input ("L" : Station connect)
26	AVIN	I	No function (Constant "H")
27	$\overline{\text{LDON}}$	O	Laser diode control output ("L" : Laser diode ON)
28	$\overline{\text{XRST}}$	O	Digital servo IC and external CD signal treatment IC reset output
29	$\overline{\text{XLAT}}$	O	Digital servo IC control serial data latch output
30	SLCK	O	Clock output for SENS serial data input.
31	TUNER	I	TV tuner connect signal input ("H" : TV tuner connect)
32	KEYLED	O	Key LED control
33	VSS	—	GND
34	$\overline{\text{SVTST1}}$	I	No function (Constant "L")
35	$\overline{\text{SVTST2}}$	I	No function (Constant "L")
36	$\overline{\text{TOUT}}$	O	GPS test mode setting control output (N-ch open drain)
37	TDATA	O	Not used.
38	TLAT	O	Not used.
39	TCLK	O	Not used.
40	CPUSTP	O	System STOP signal output
41	VSTAT	O	TV tuner/VIDEO IN select at monitor external input.
42	VNAVI	O	NAVI system/external input select on monitor.
43	DSPDAC	O	DSP IC DATA signal select output
44	SYNCCHK	I	AUX video sync. detect input ("H" : Video sync. input available)
45	AUXSON	O	TV tuner SIRCS signal control output ("H" : SIRCS output to TV tuner)
46	BEEP	O	BEEP output

Pin No.	Pin Name	I/O	Pin Description
47	DIMMER	O	LCD display DIMMER output ("H" : DIMMER ON (dark), "L" : DIMMER OFF (bright))
48	VMUTE	O	Visual mute control output ("H" : Mute ON) (Not used in this set.)
49	AMUTE	O	Audio mute control output ("H" : Mute ON)
50	RGBMUT	O	Analog RGB MUTE output ("H" : Analog RGB MUTE ON, "L" : Analog RGB MUTE OFF)
51	DACMUT	O	DAC AUDIO MUTE output ("H" : DAC AUDIO MUTE OFF, "L" : DAC AUDIO MUTE ON)
52	ASTAT	O	Audio output select ("L" : TV tuner, "H" : station Aux, "–" : CD, DSP)
53	ANAVI	O	Audio output select ("L" : TV tuner, "L" : station Aux, "H" : CD, DSP)
54	SVPW	O	CD driver IC control ("L" : CD driver IC standby mode)
55	$\overline{\text{BUSON}}$	O	NAVI-BUS ON/OFF control output ("H" : NAVI-BUS OFF, "L" : NAVI-BUS ON)
56	SYSPW	O	System power control output ("H" : System power ON, "L" : System power OFF)
57	DISPPW	O	Display power control output ("H" : Display power ON, "L" : Display power OFF)
58	RSTSW	I	RESET condision input ("H" : RESET switch ON, "L" : RESET IC ON)
59	$\overline{\text{NVRST}}$	O	System reset control output
60	$\overline{\text{RESET}}$	I	Micro computer reset input
61	SIRCS	I	Remote commander signal (SIRCS) input
62	BUCHK	I	Backup power level detection input ("H" : Backup ON, "L" : Backup OFF)
63	$\overline{\text{ACCCHK}}$	I	Accessory switch (Acc sw.) detection input ("H" : Acc sw. OFF, "L" : Acc sw. ON)
64	$\overline{\text{PWSW}}$	I	POWER button input
65	CDOPN	I	CD lid OPEN switch input
66	SCOR	I	Sub code sync input
67	P06/INTP6	I	DISC insert detection switch input (Not used in this set.)
68	VDD	—	Power supply pin (+5 V)
69	X2		Crystal oscillator for main system clock oscillation (4.9152 MHz).
70	X1		Crystal oscillator for main system clock oscillation (4.9152 MHz).
71	IC	—	GND
72	XT2		Crystal oscillator for sub system clock oscillation. (Not used in this set.)
73	DEBUG	I	Debug mode select switch input (Fixed at "L" in this set.)
74	AVDD	—	A/D converter analog power pin (+5 V)
75	AVREF	—	A/D converter reference voltage pin (+5 V)
76	TEMPL	I	Temperature detection (Low temperature) thermistor voltage input
77	TEMPH	I	Temperature detection (High temperature) thermistor voltage input
78, 79	MOVE0, MOVE1	I	Operation sensor A/D converter input
80	LOWVOL	I	Reducing voltage check input

• **IC Block Diagrams**

IC1 M51406FP



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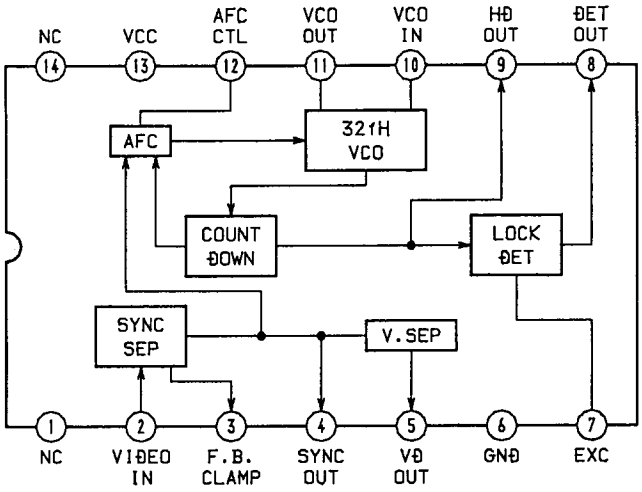

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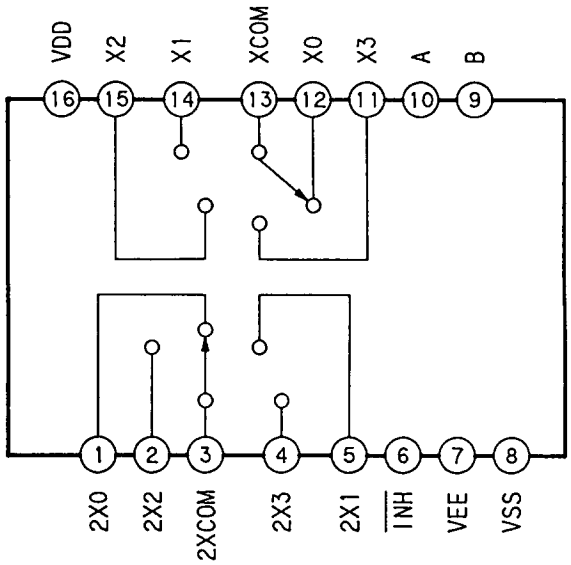

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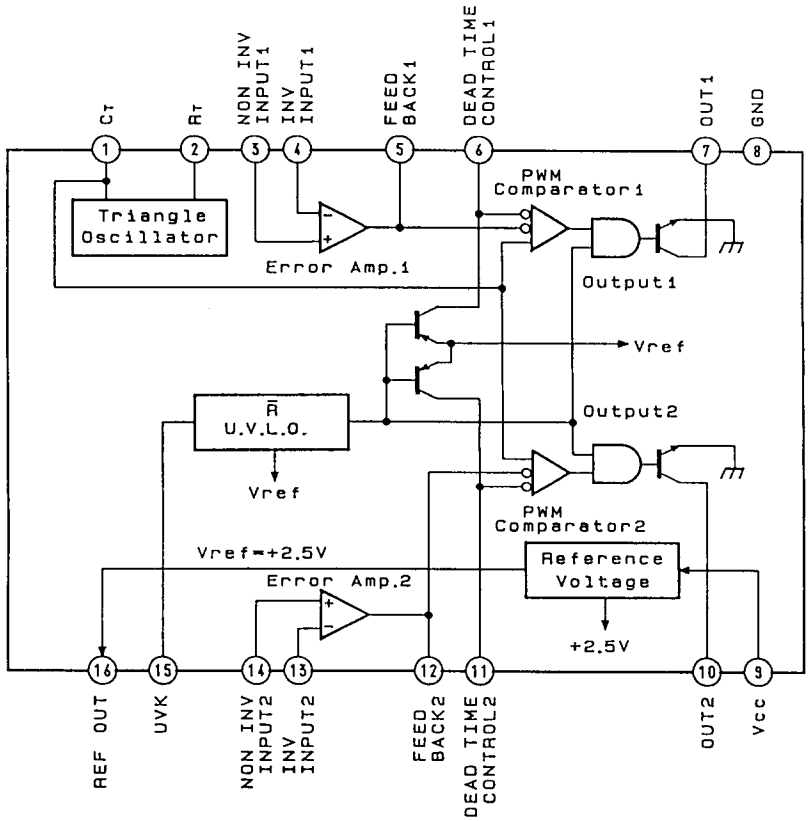

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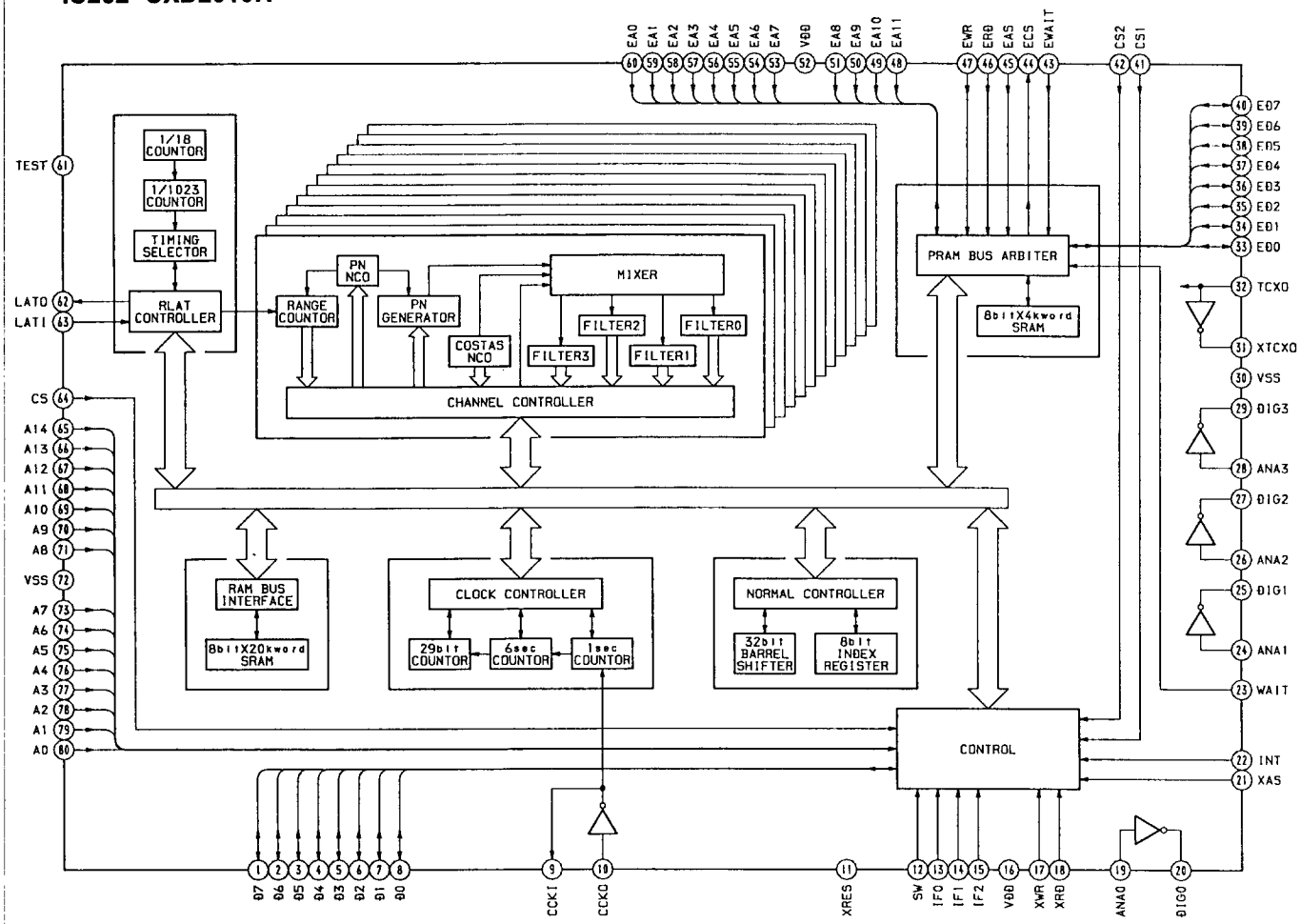
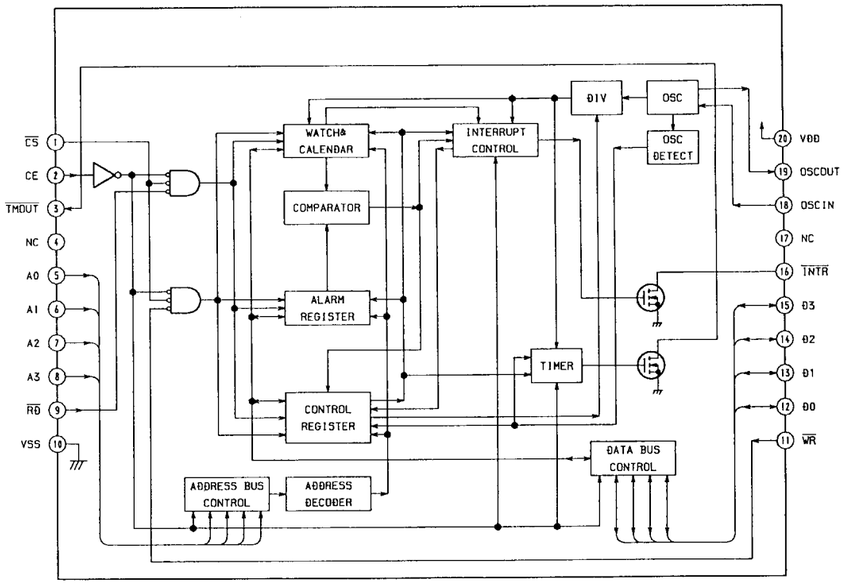


IC203 RS5C62-E2



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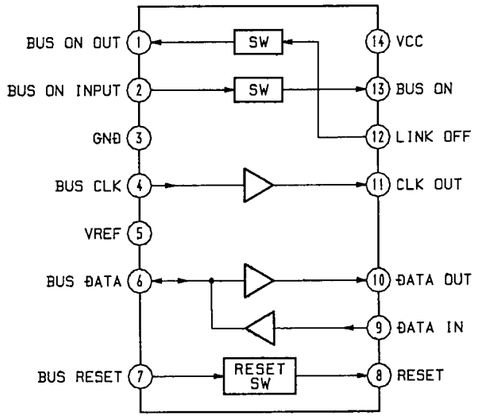

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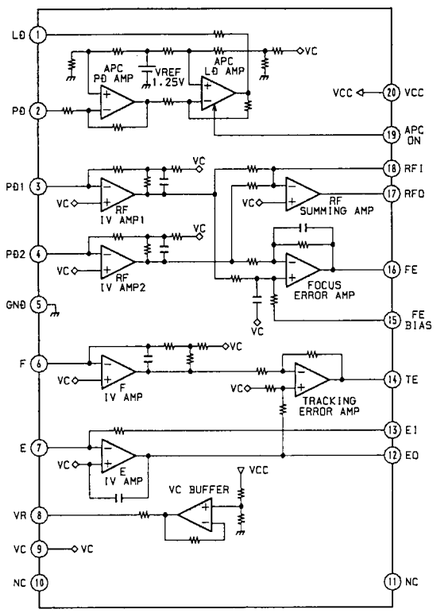

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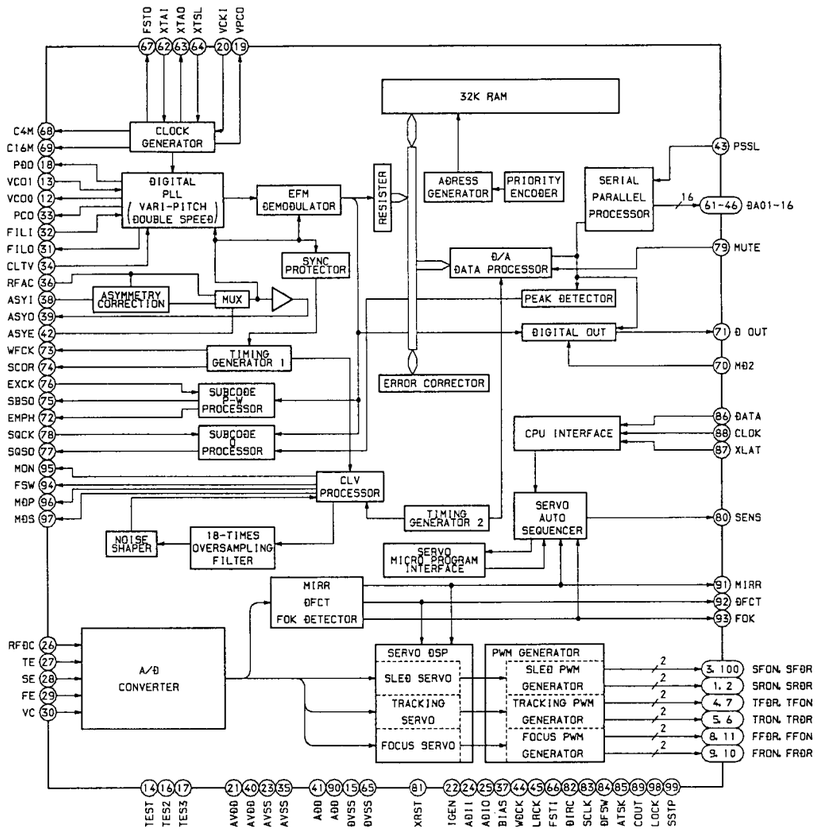

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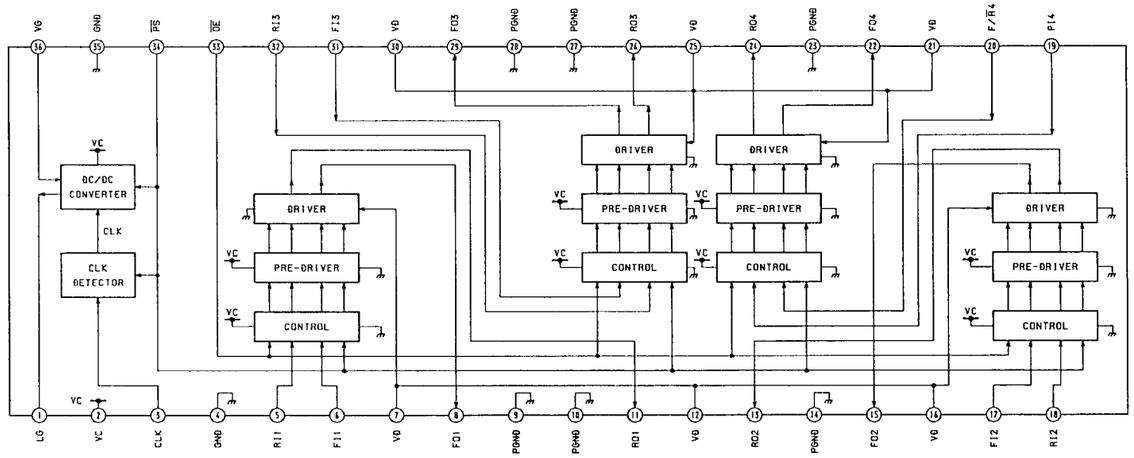

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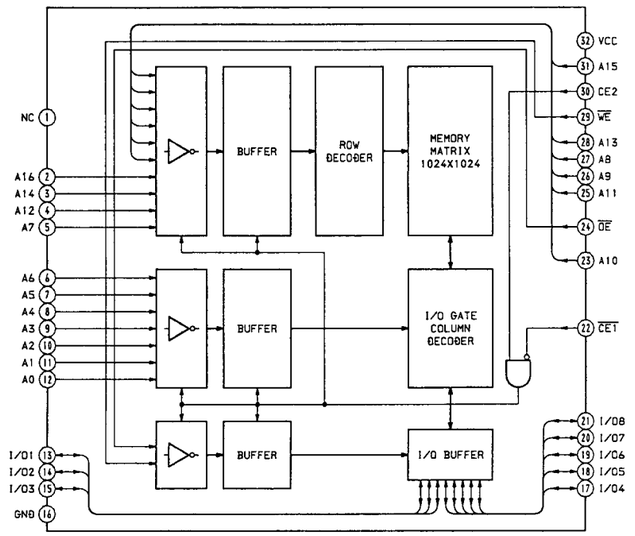

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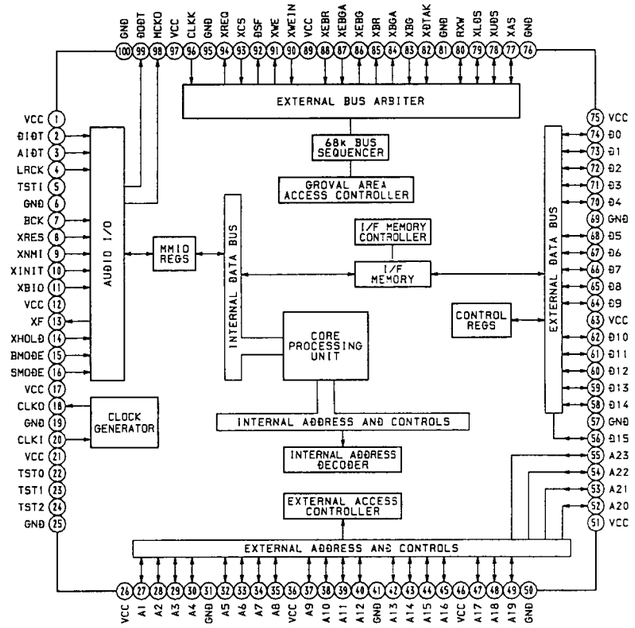

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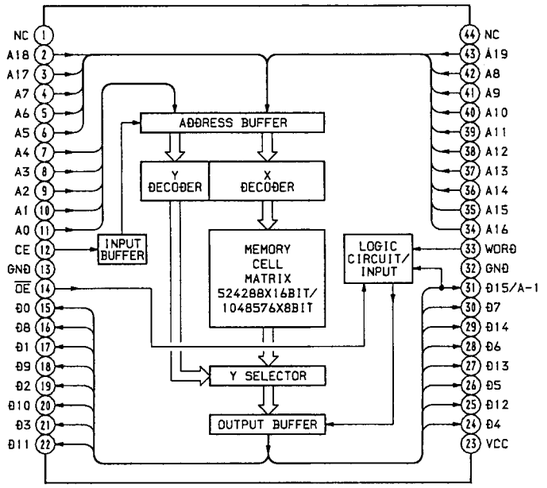

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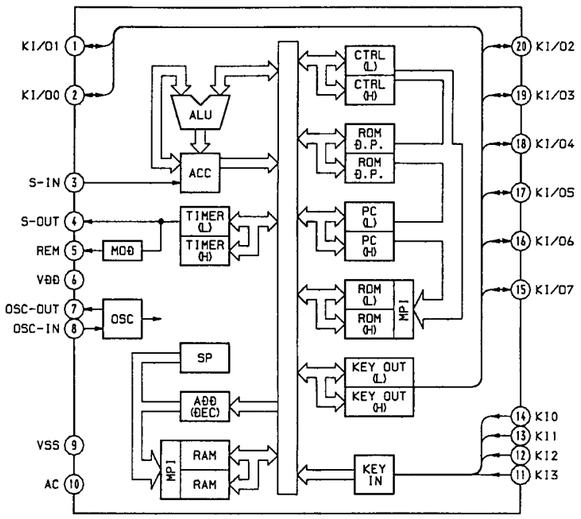

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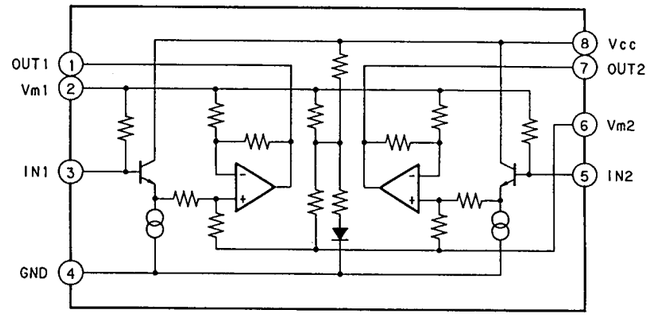

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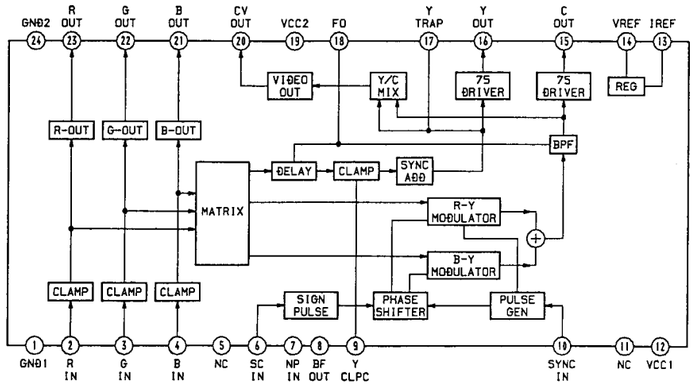

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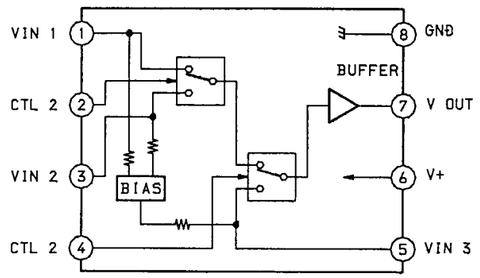

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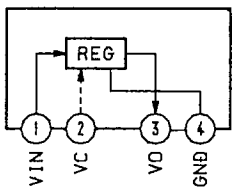
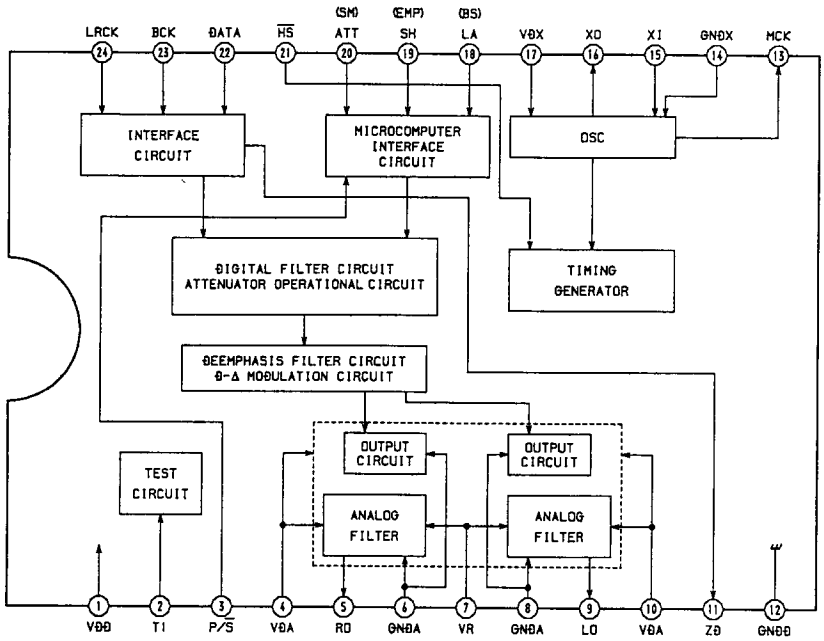
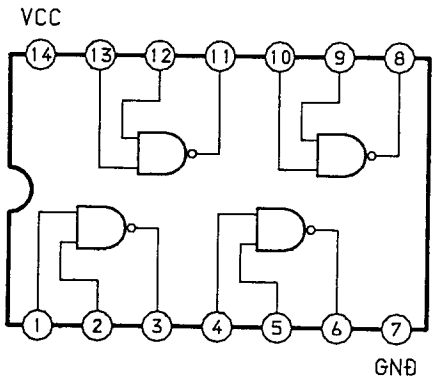


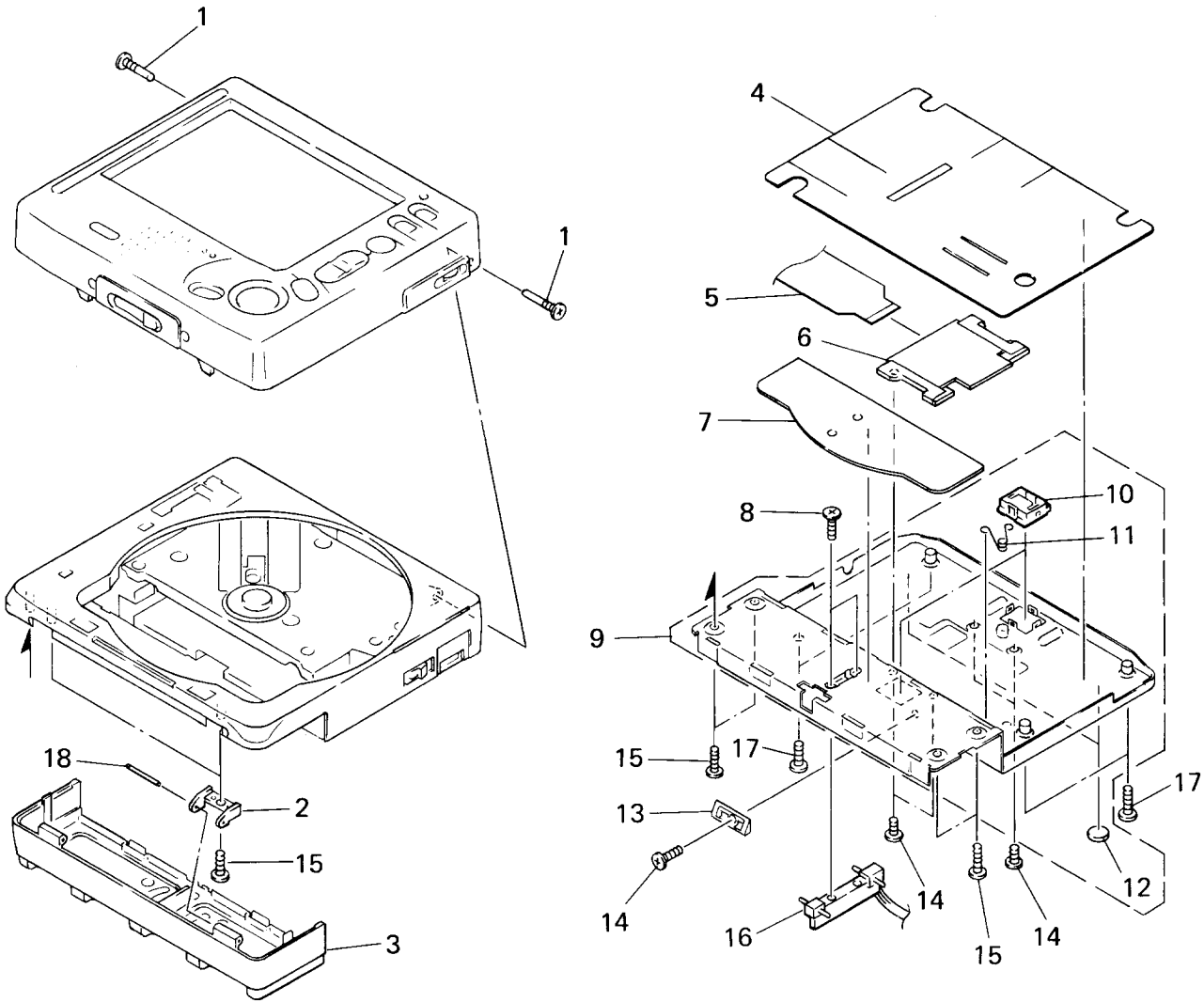
IC909 TC9404FN-EL



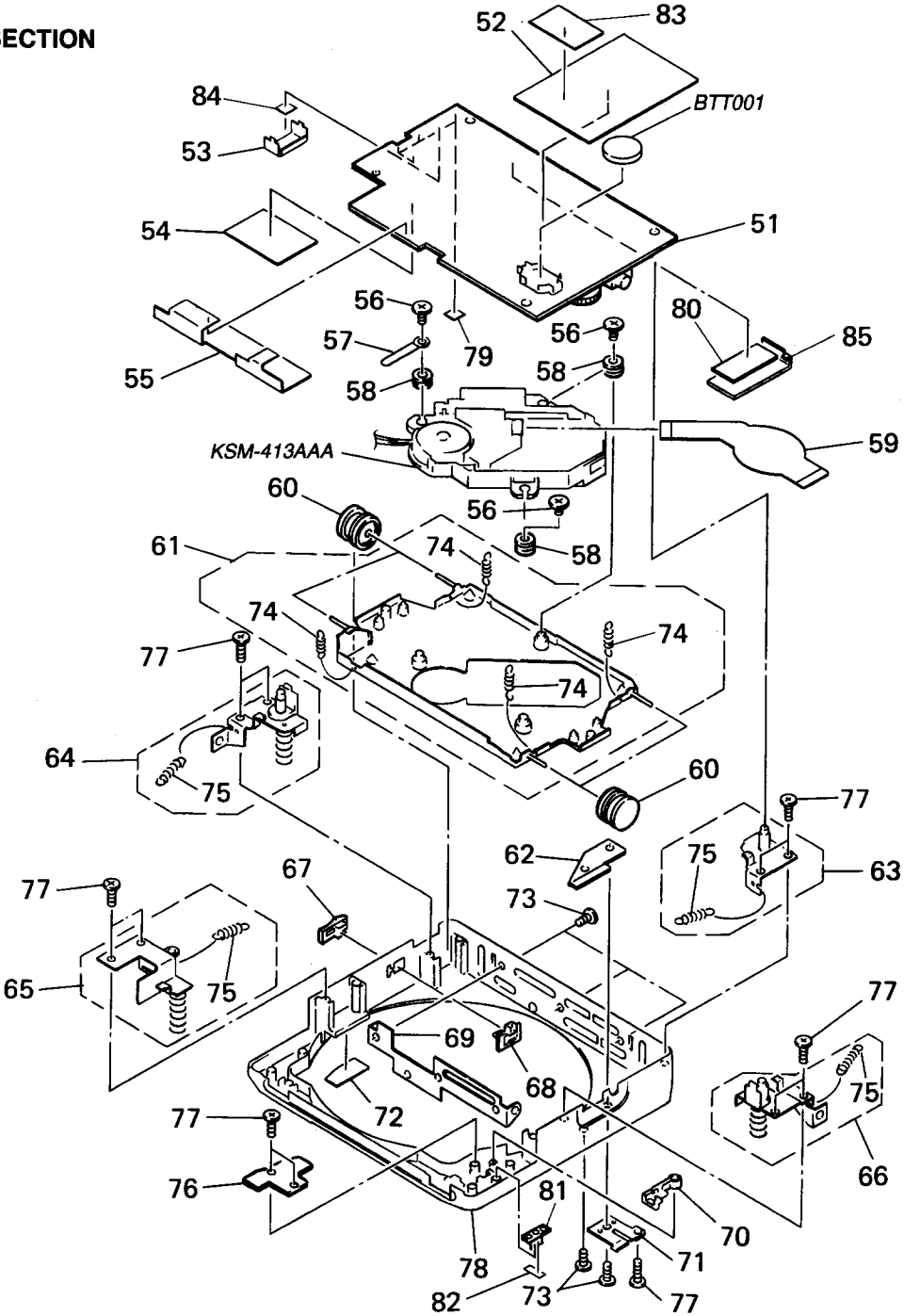
IC910 SN74HC00ANS



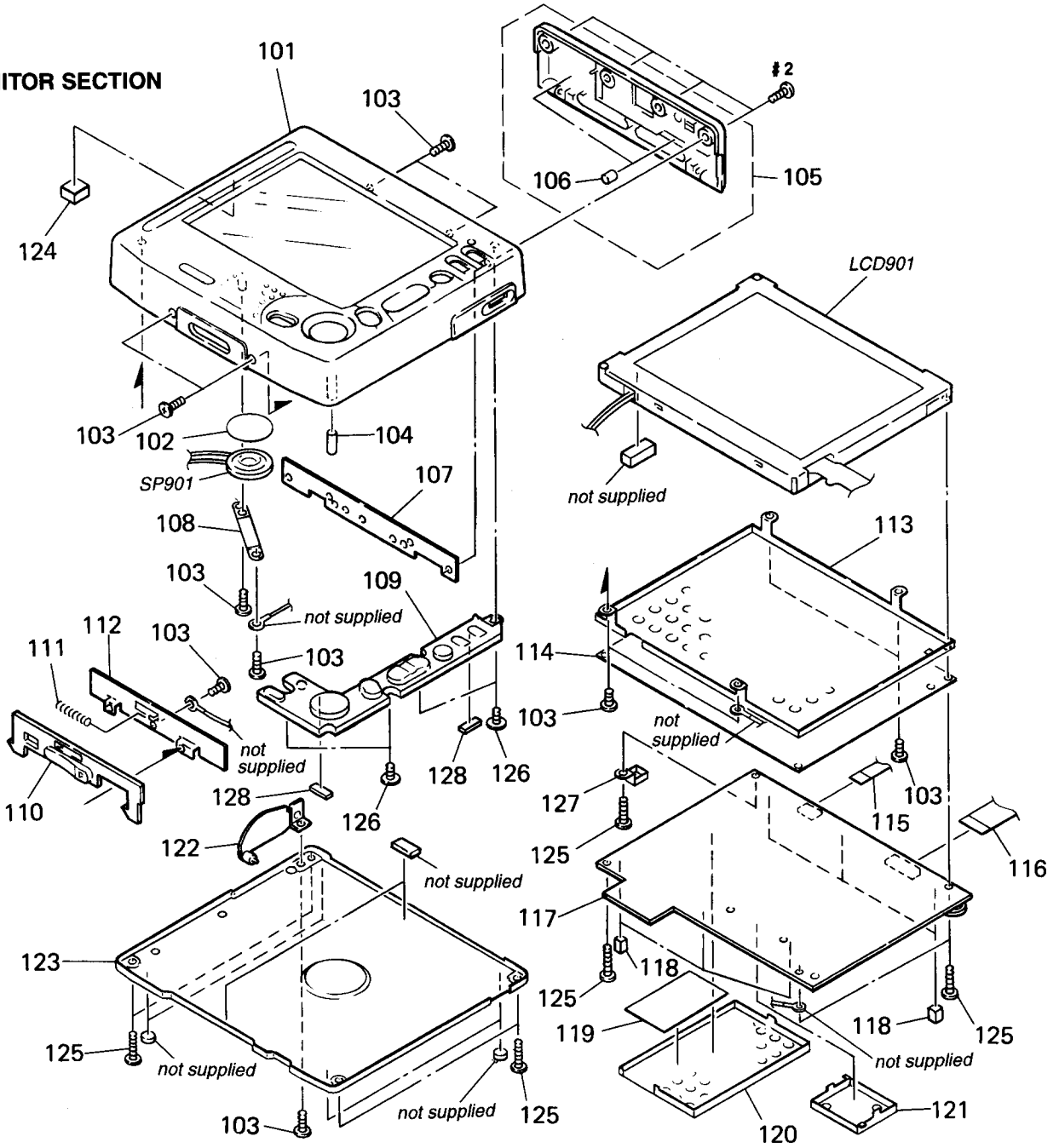
5-1. BOTTOM PLATE SECTION



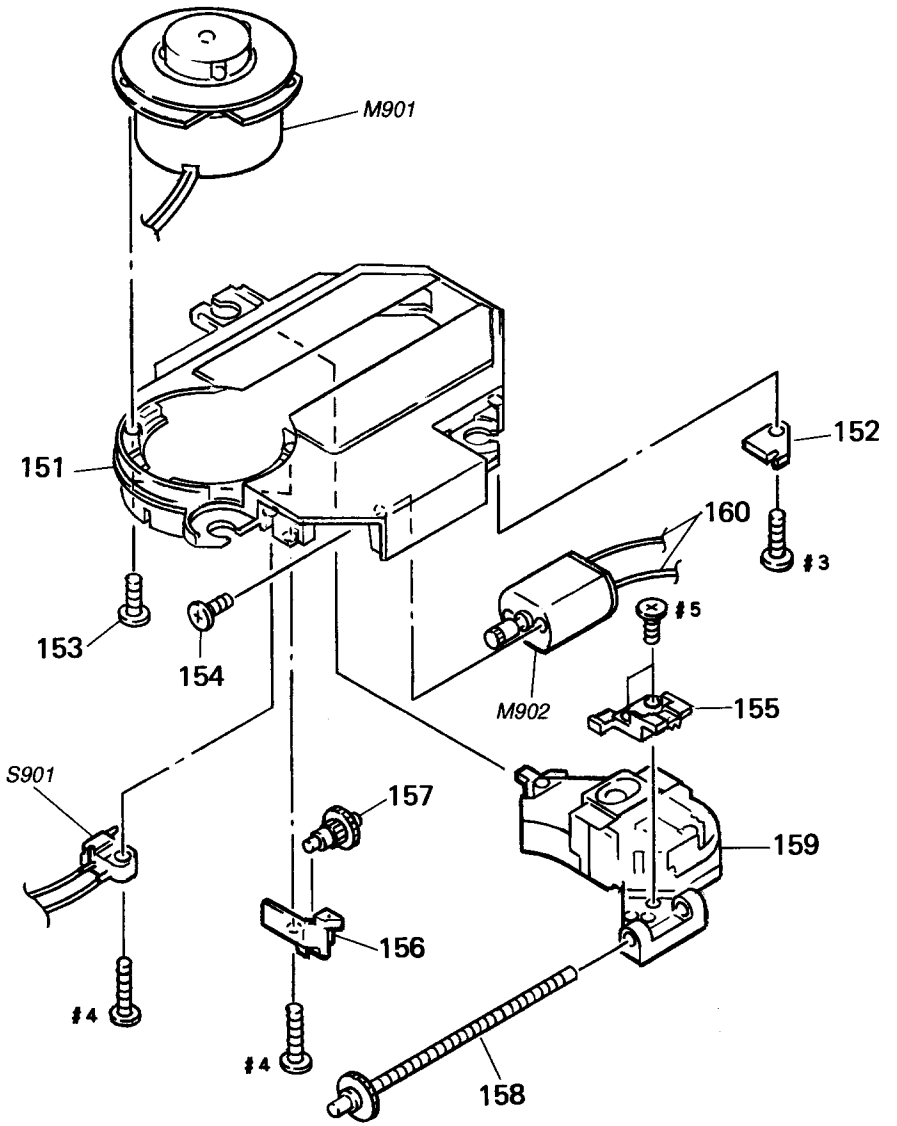
5-2. CD ROM SECTION



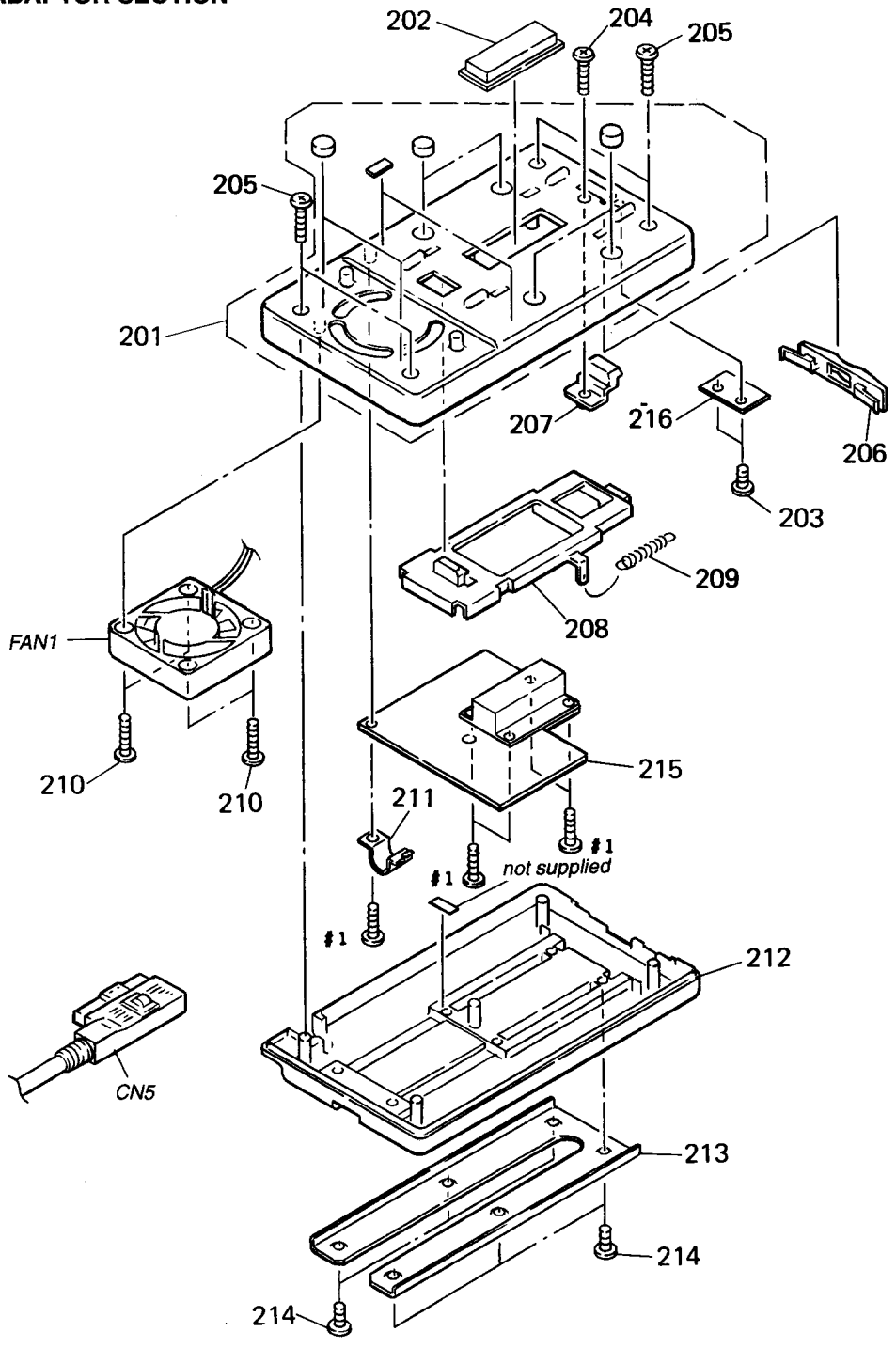
5-3. MONITOR SECTION



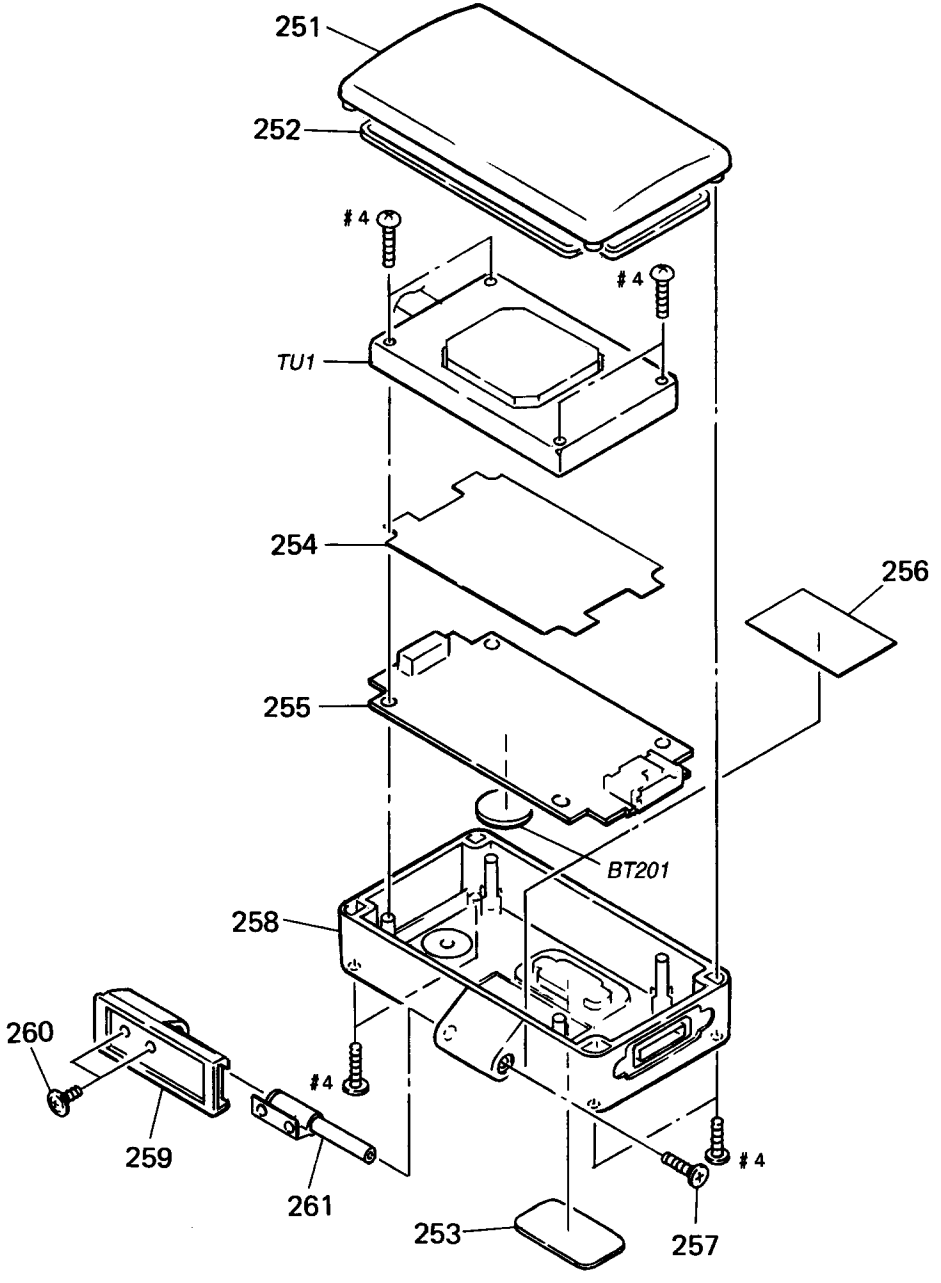
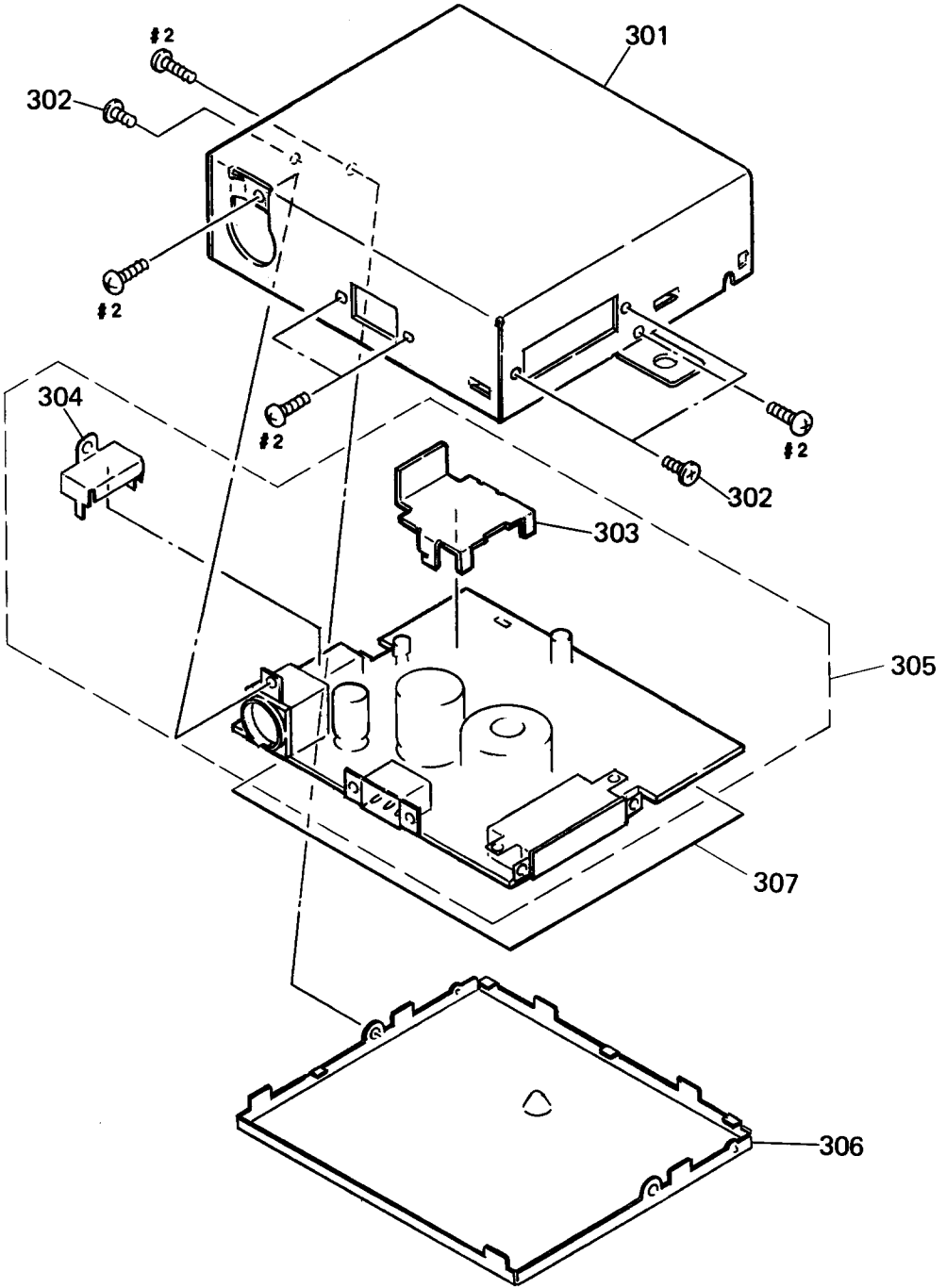
5-4. OPTICAL PICK-UP SECTION
(KSM-413AAA)



5-5. CAR MOUNT ADAPTOR SECTION



5-6. GPS ANTENNA SECTION



5-7. CONNECTION BOX SECTION